

MODEL NAME : PAR10

PCB NO : LA-6571P (DA80000K510)

BOM P/N : 43194731L01→R1 BOM, PCH: (SA00004ED5L) SLJ4N B3
43194731L03→R3 BOM, PCH: (SA00004ED6L) SLJ4N B3

Compal Confidential

Avenger

www.alttech1.ru

rPGA Sandy Bridge + FCBGA PCH Cougar Point-M + MXM x2

Rev: 1.0 (A00)

2011.03.15

@ : Nopop component

CONN@ : ME connector

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Project Code : PAR10
File Name : LA-6571P



Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF		LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State	power plane	+1.5V	+5VS
	+5VALW +3VALW +3VLP +3V_PCH		+3VS +1.8VS +1.5VS +0.75VS +3VMXM +5VMXM +VCCP +VCCSA +VCC_CORE +1.5V_CPU_VDDQ
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

USB

USB PORT#	DESTINATION
0	JUSB1
1	JUSB2
2	EXPRESS CARD
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (DMC)
6	AlienFX/ELC
7	None
8	Bluetooth
9	JESATA
10	None
11	None
12	None
13	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	CLK_14M
	CLKOUT_PCIE2	MINI CARD-2 DMC	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	EXPRESS CARD		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	MXM I		
	CLKOUT_PEG_B	MXM II		

Symbol Note :



Digital Ground



Analog Ground

SATA	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	None
SATA4	ESATA
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	EXPRESS CARD
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	None
PCI4	None

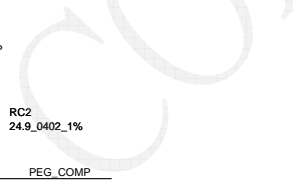
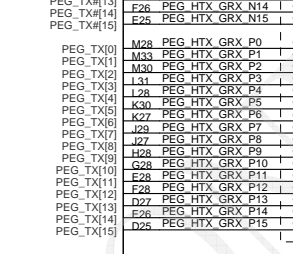
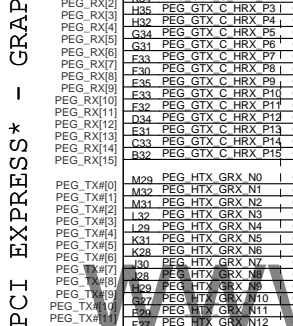
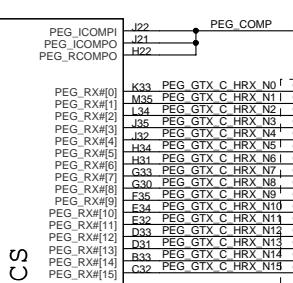
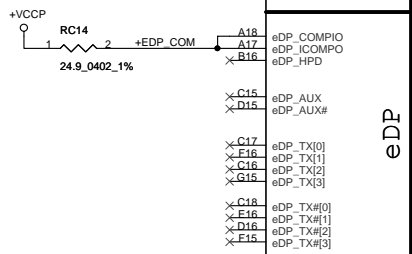
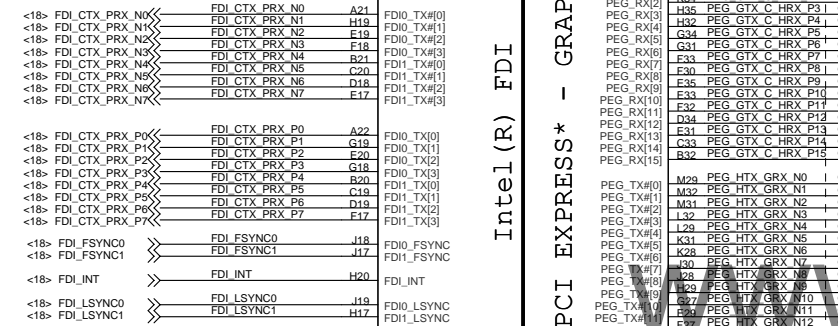
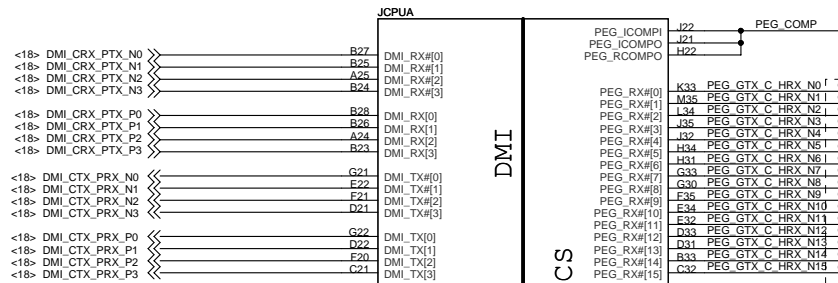
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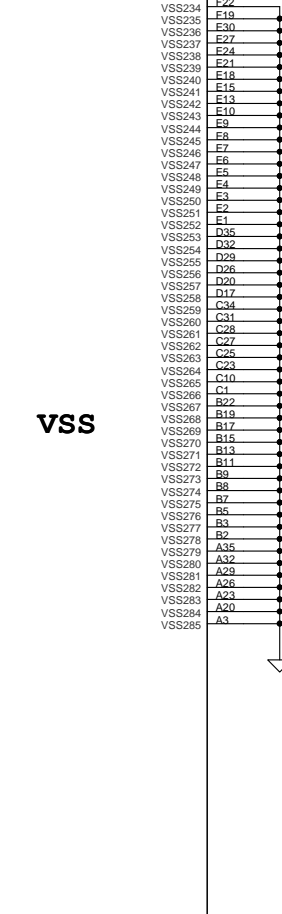
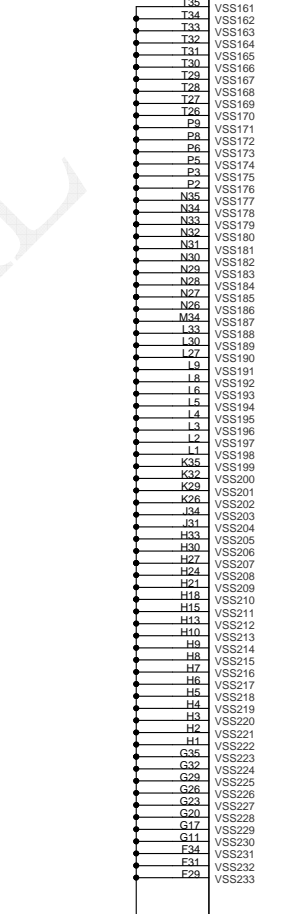
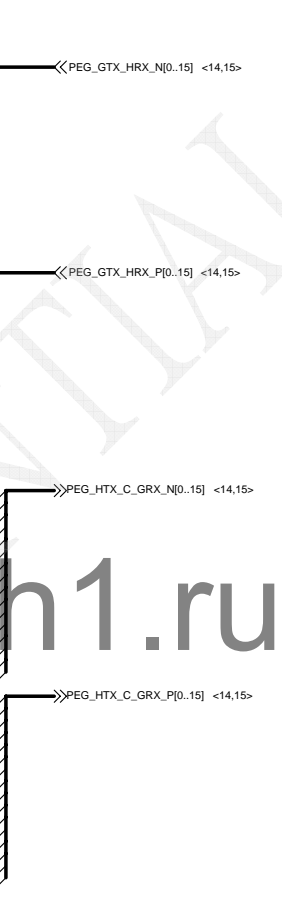
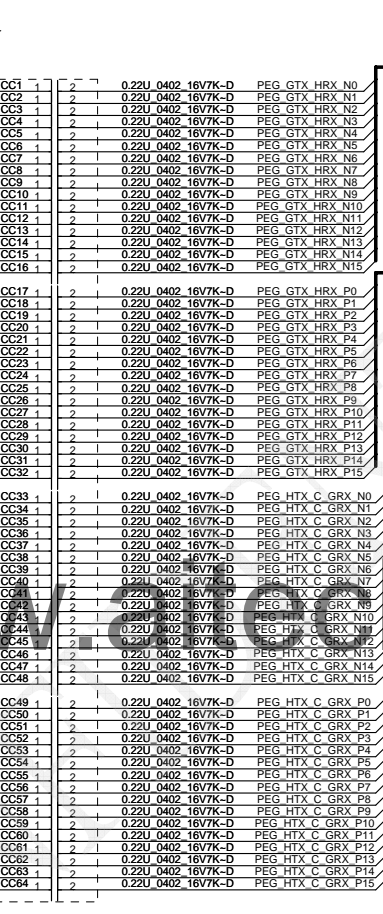
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PEG ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms

PEG ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



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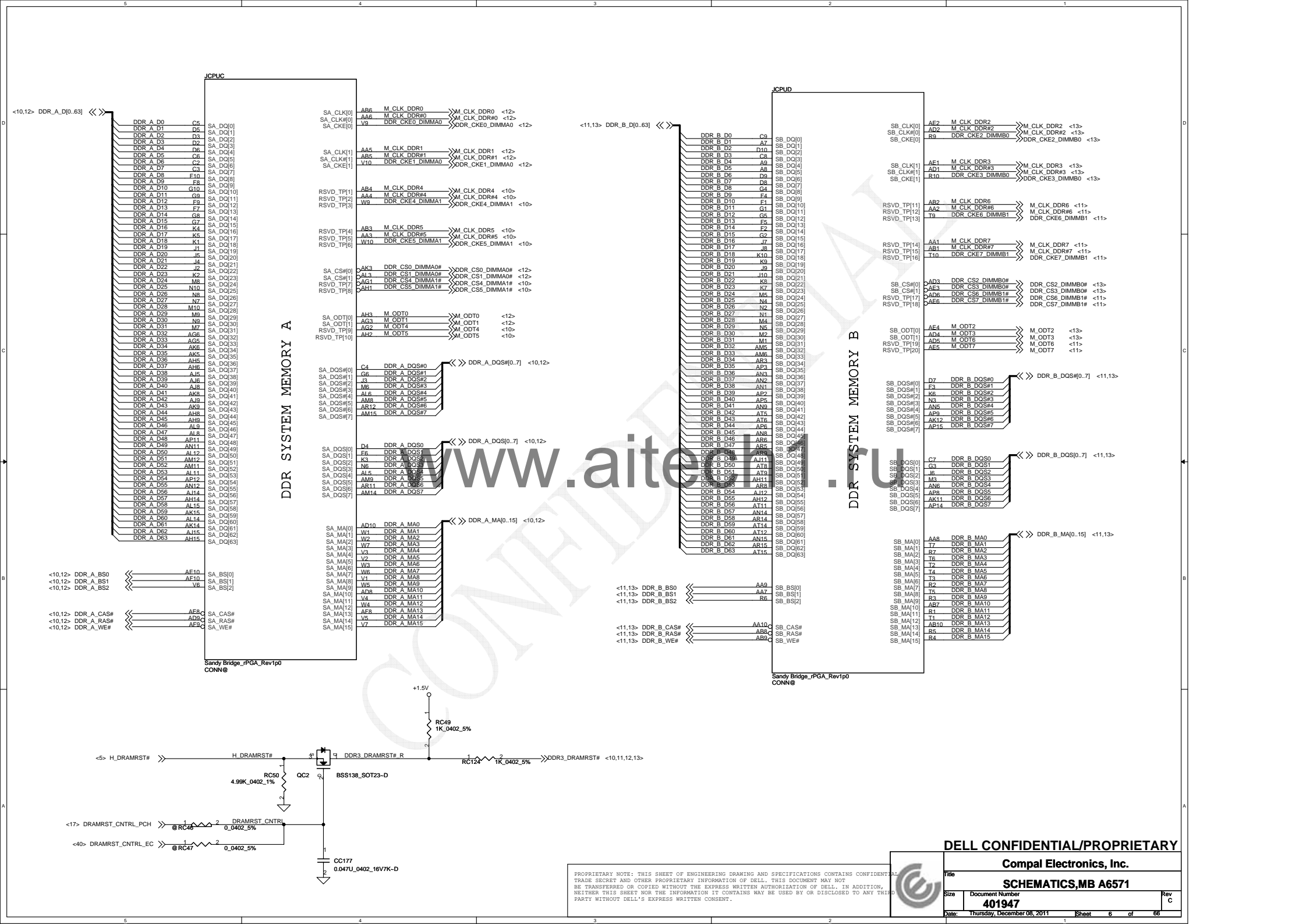
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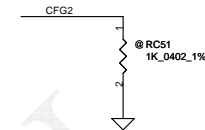
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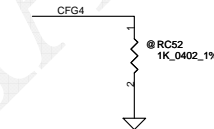
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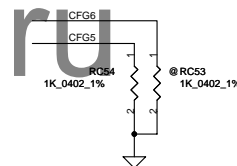
CFG Straps for Processor



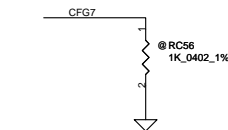
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training

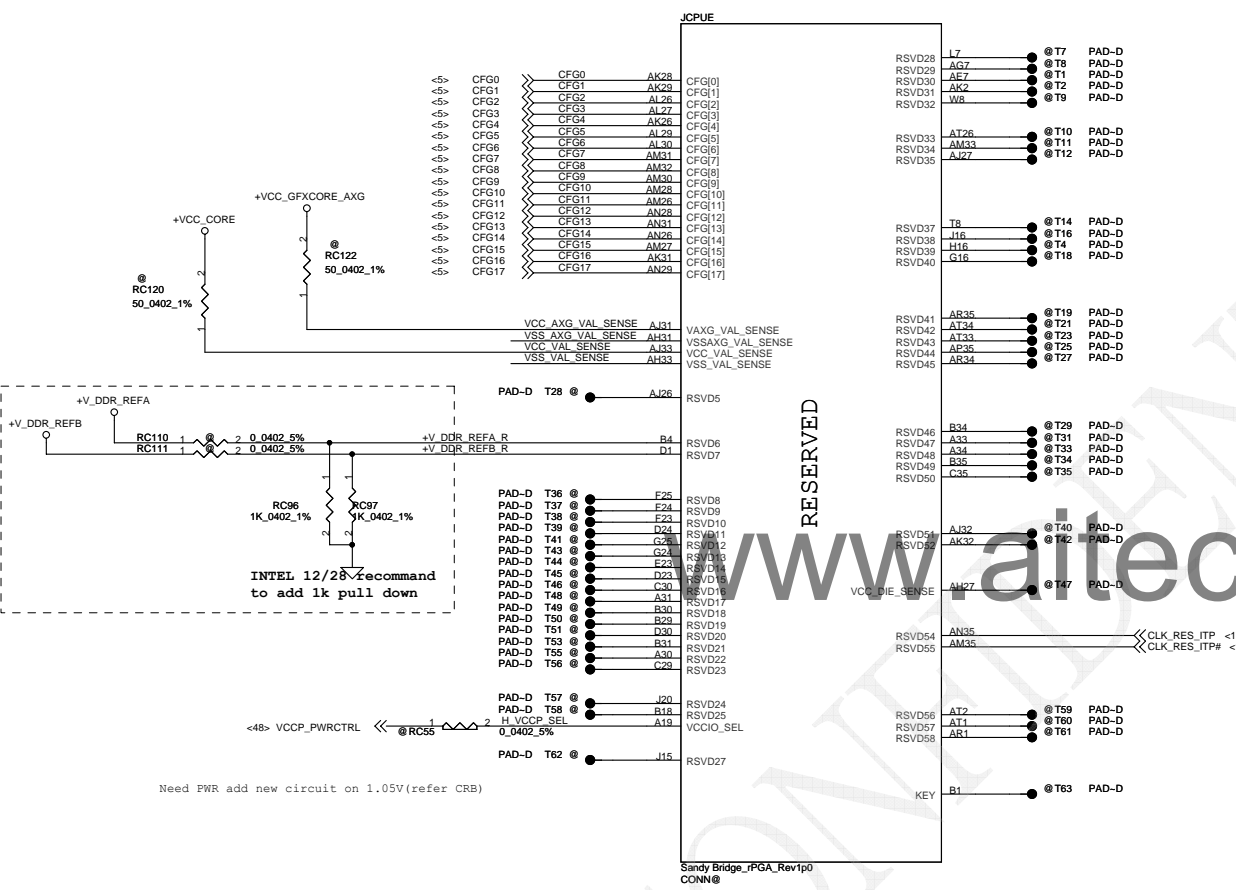
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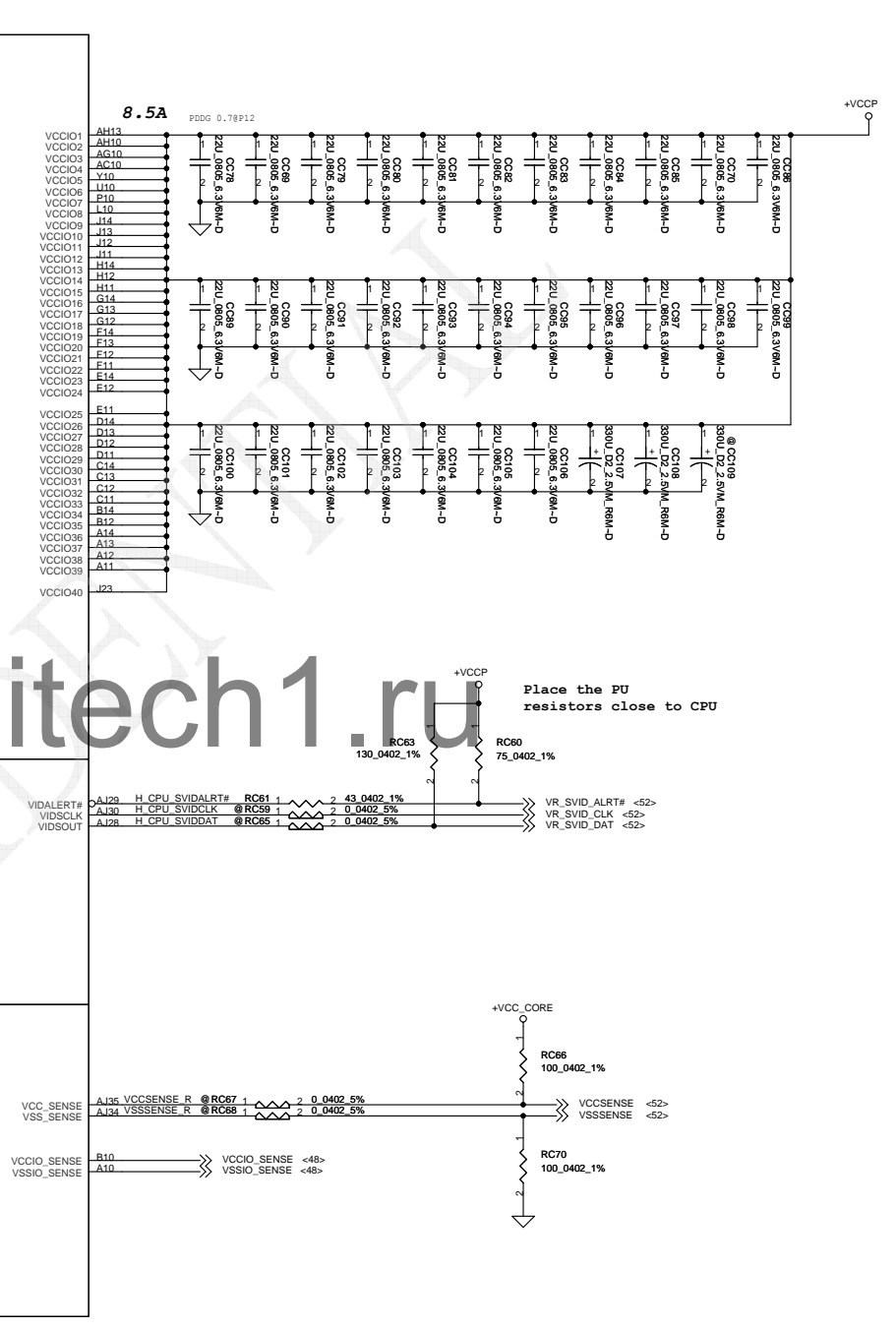
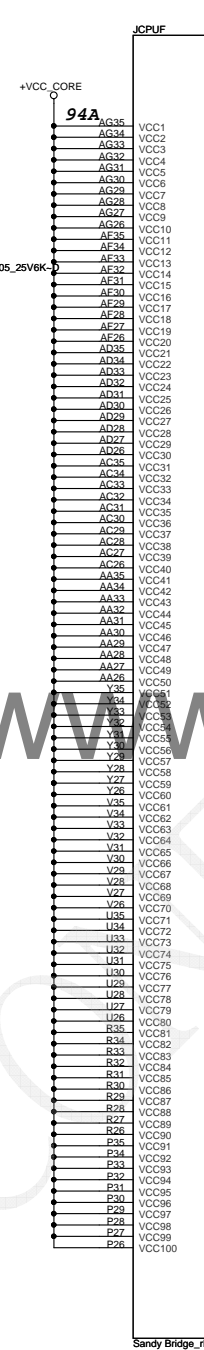
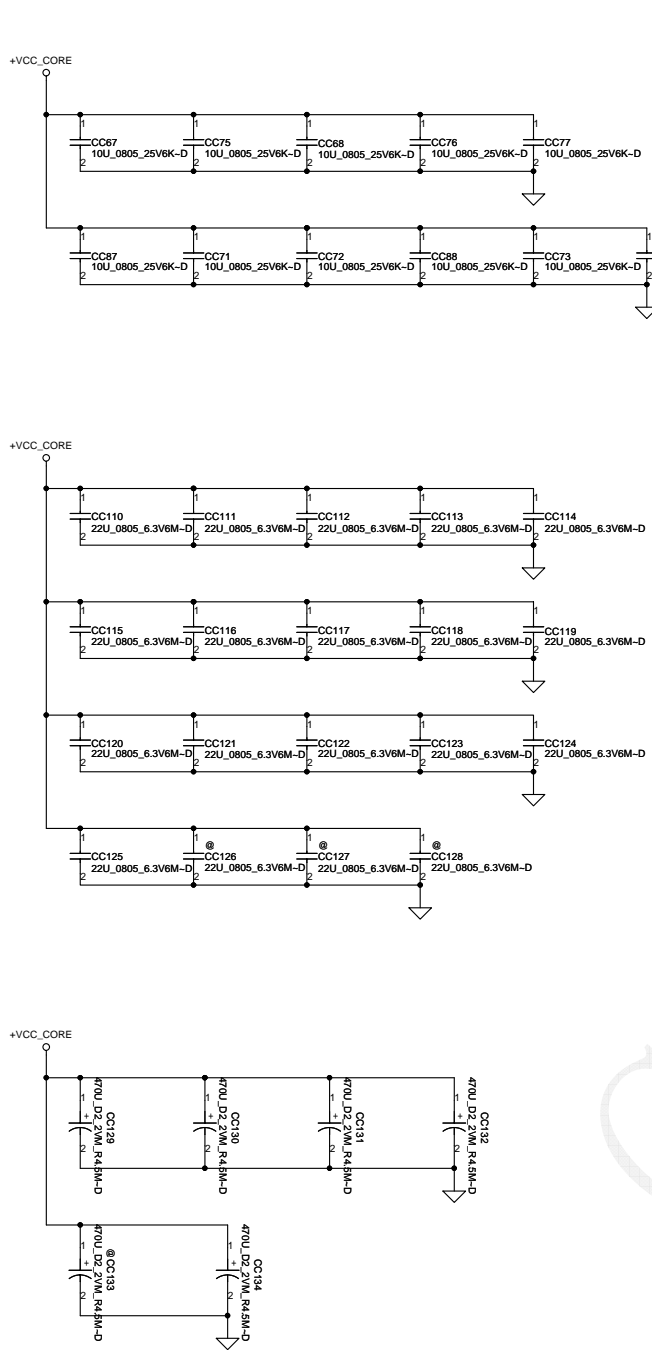
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INTEL 12/28 recommend
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1



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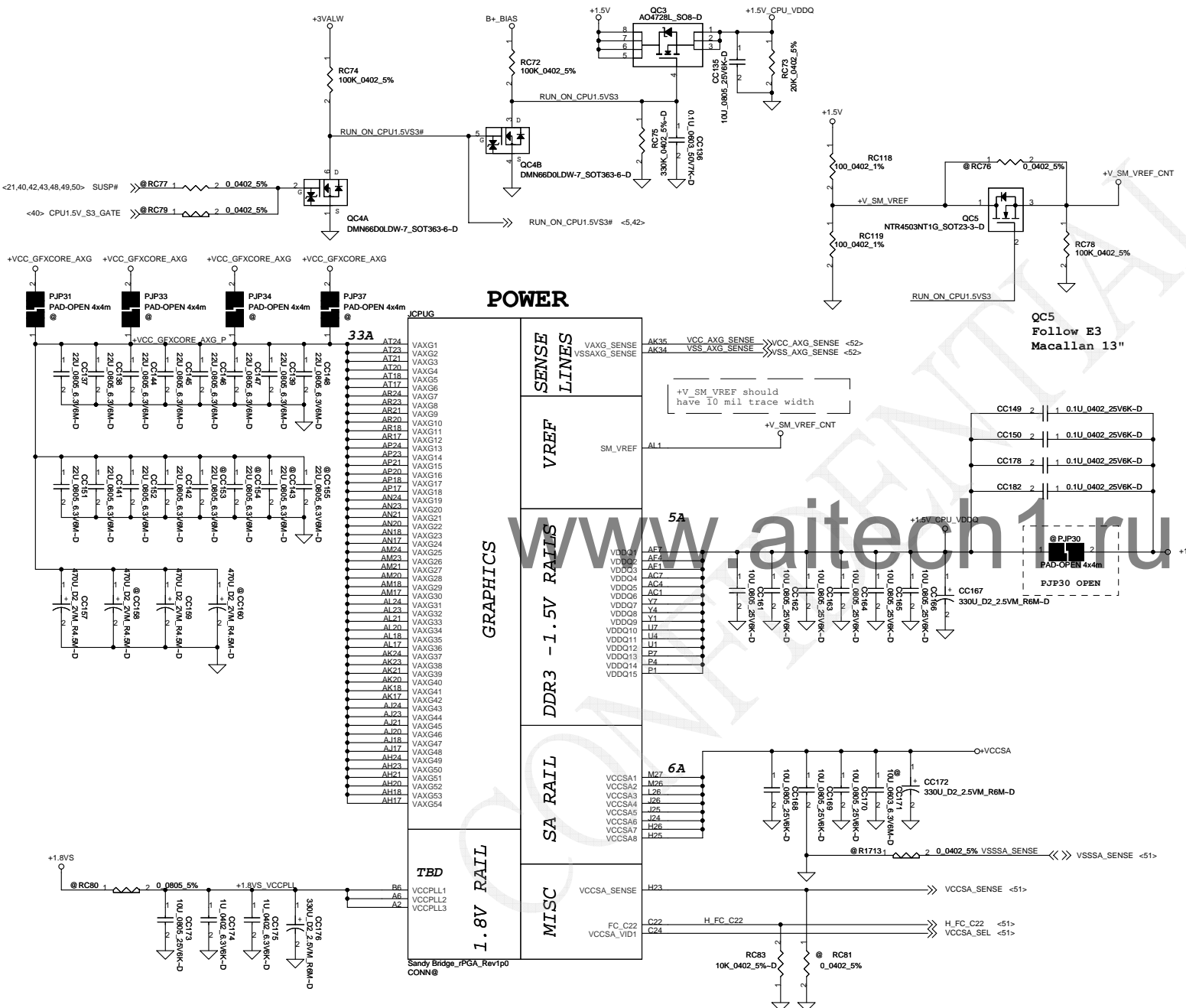
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+1.5V_CPU_VDDQ Source



JCPUH	
AT35	VSS1
AT32	VSS2
AT29	VSS3
AT27	VSS4
AT25	VSS5
AT22	VSS6
AT19	VSS7
AT16	VSS8
AT13	VSS9
AT10	VSS10
AT7	VSS11
AT4	VSS12
AT1	VSS13
AT22	VSS14
AT19	VSS15
AT16	VSS16
AT13	VSS17
AT10	VSS18
AT7	VSS19
AT4	VSS20
AT1	VSS21
AT22	VSS22
AT19	VSS23
AT16	VSS24
AT13	VSS25
AT10	VSS26
AT7	VSS27
AT4	VSS28
AT1	VSS29
AT22	VSS30
AT19	VSS31
AT16	VSS32
AT13	VSS33
AT10	VSS34
AT7	VSS35
AT4	VSS36
AT1	VSS37
AT22	VSS38
AT19	VSS39
AT16	VSS40
AT13	VSS41
AT10	VSS42
AT7	VSS43
AT4	VSS44
AT1	VSS45
AT22	VSS46
AT19	VSS47
AT16	VSS48
AT13	VSS49
AT10	VSS50
AT7	VSS51
AT4	VSS52
AT1	VSS53
AT22	VSS54
AT19	VSS55
AT16	VSS56
AT13	VSS57
AT10	VSS58
AT7	VSS59
AT4	VSS60
AT1	VSS61
AT22	VSS62
AT19	VSS63
AT16	VSS64
AT13	VSS65
AT10	VSS66
AT7	VSS67
AT4	VSS68
AT1	VSS69
AT22	VSS70
AT19	VSS71
AT16	VSS72
AT13	VSS73
AT10	VSS74
AT7	VSS75
AT4	VSS76
AT1	VSS77
AT22	VSS78
AT19	VSS79
AT16	VSS80

VSS

POWER

GRAPHICS

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

TBD

Sandy Bridge_rPGA_Rev1p0
CONN@

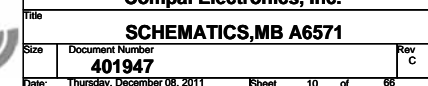
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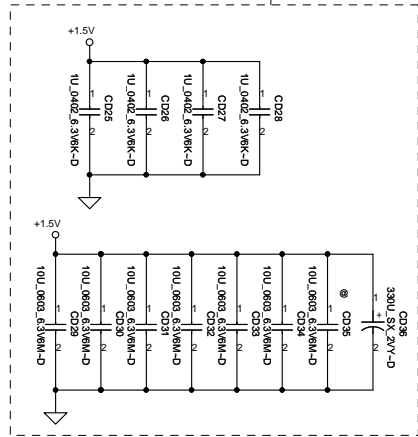
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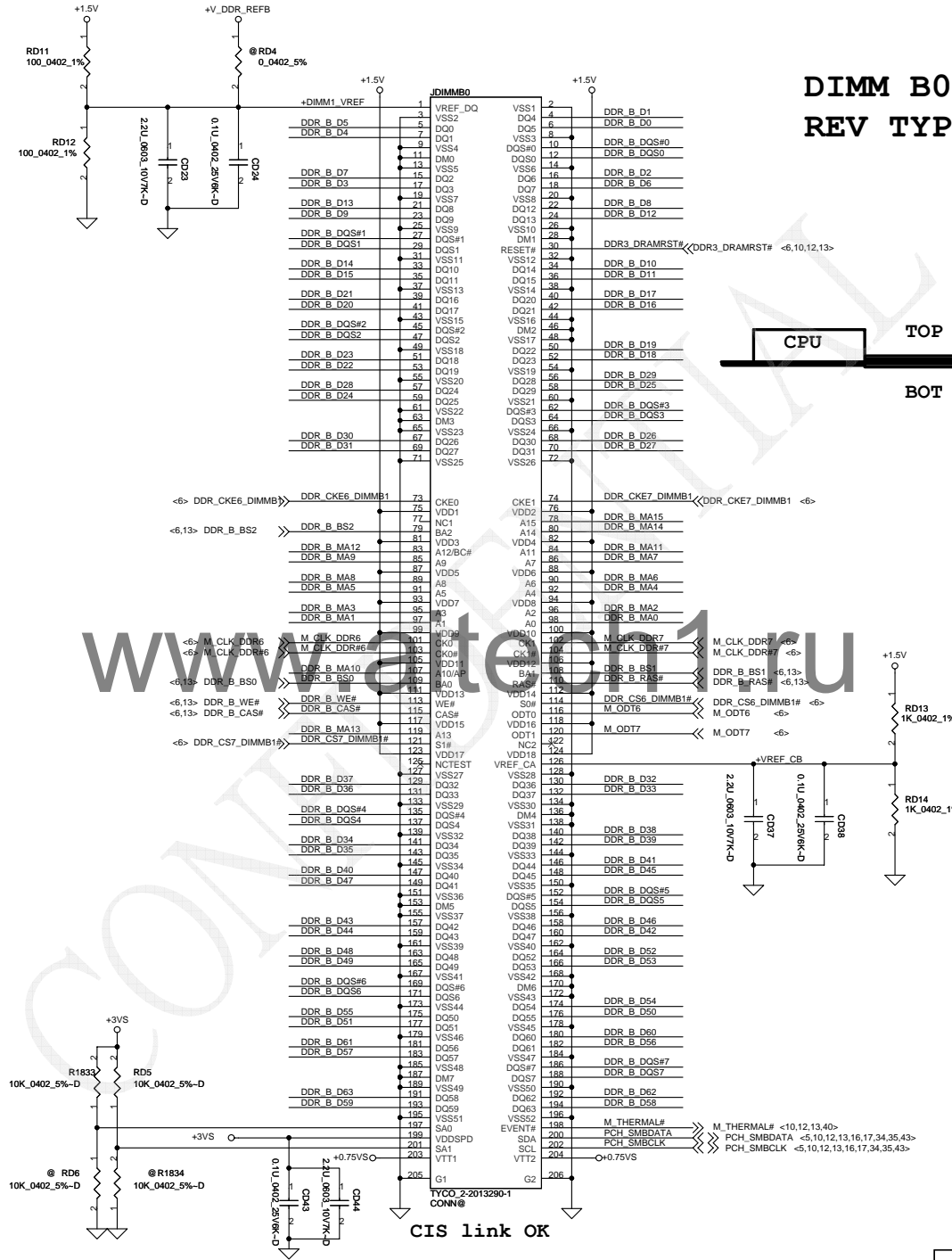
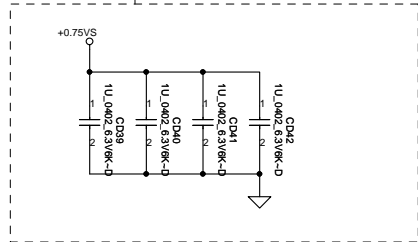


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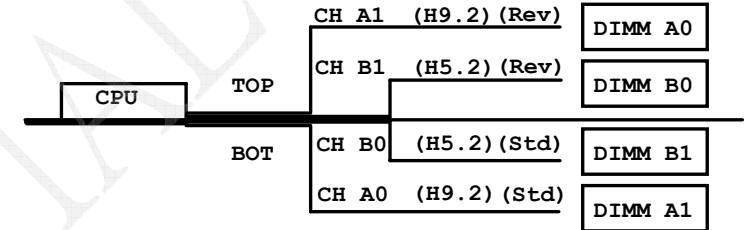
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Layout Note:
Place near JDIMMB.203,204



DIMM B0 REV TYPE (H5.2)



CIS link OK

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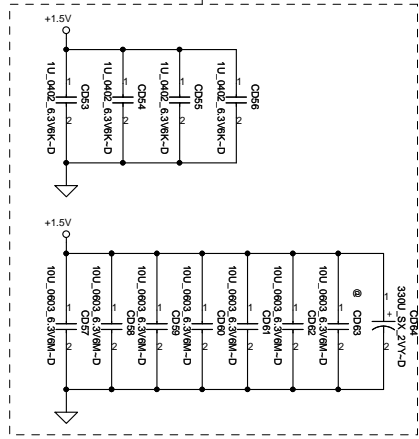
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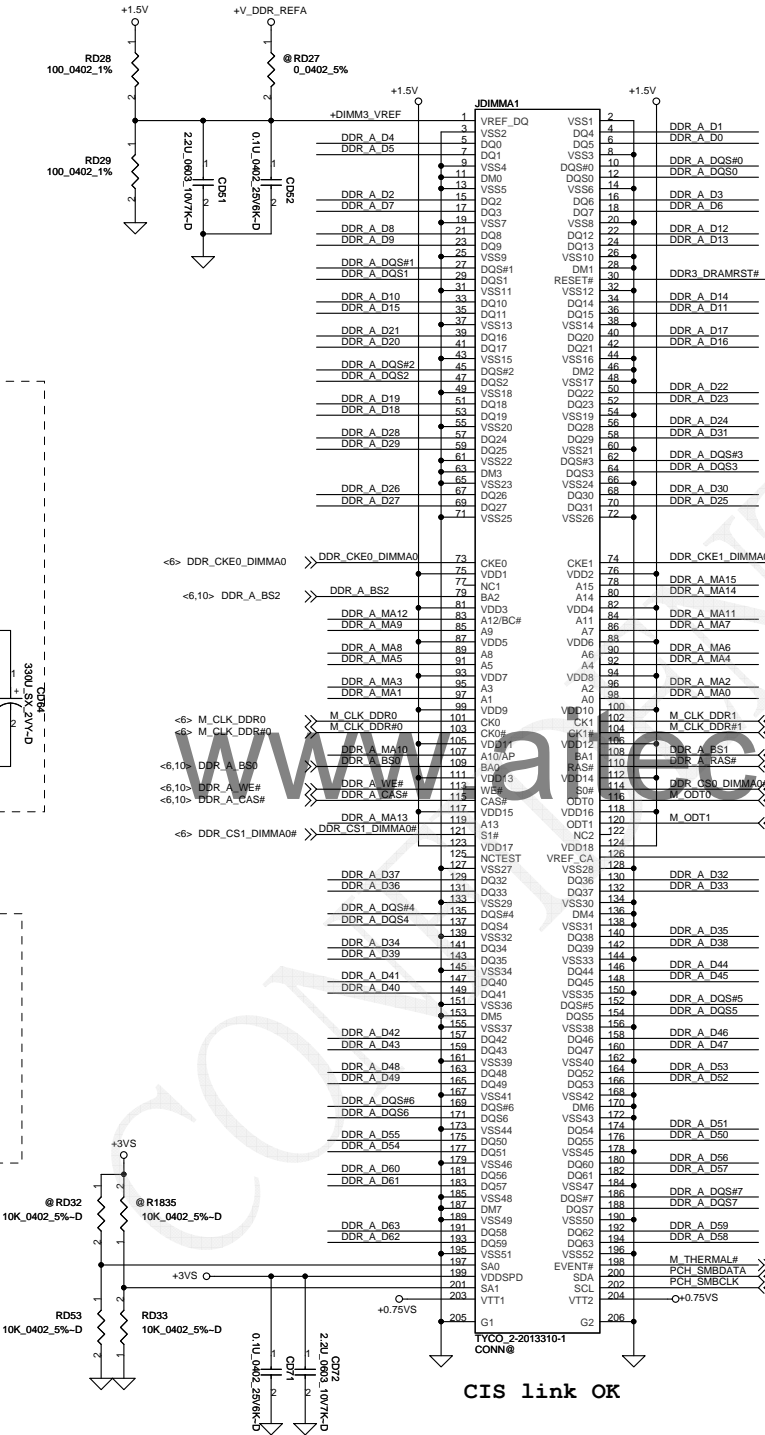
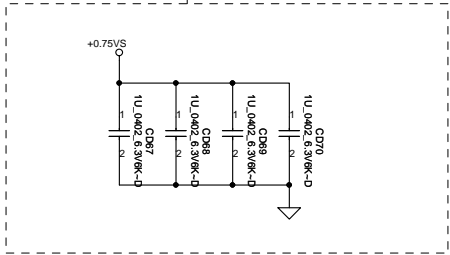
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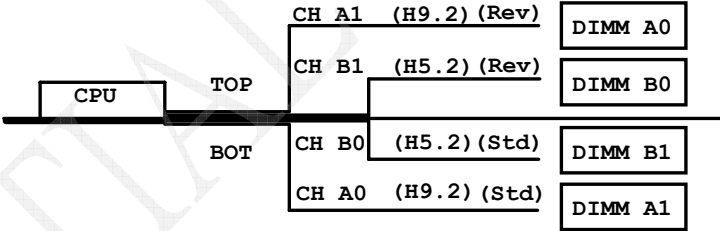
Layout Note:
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Layout Note:
Place near JDIMMC.203,204



DIMM A1 STD TYPE (H9.2)



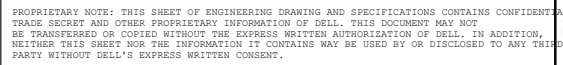
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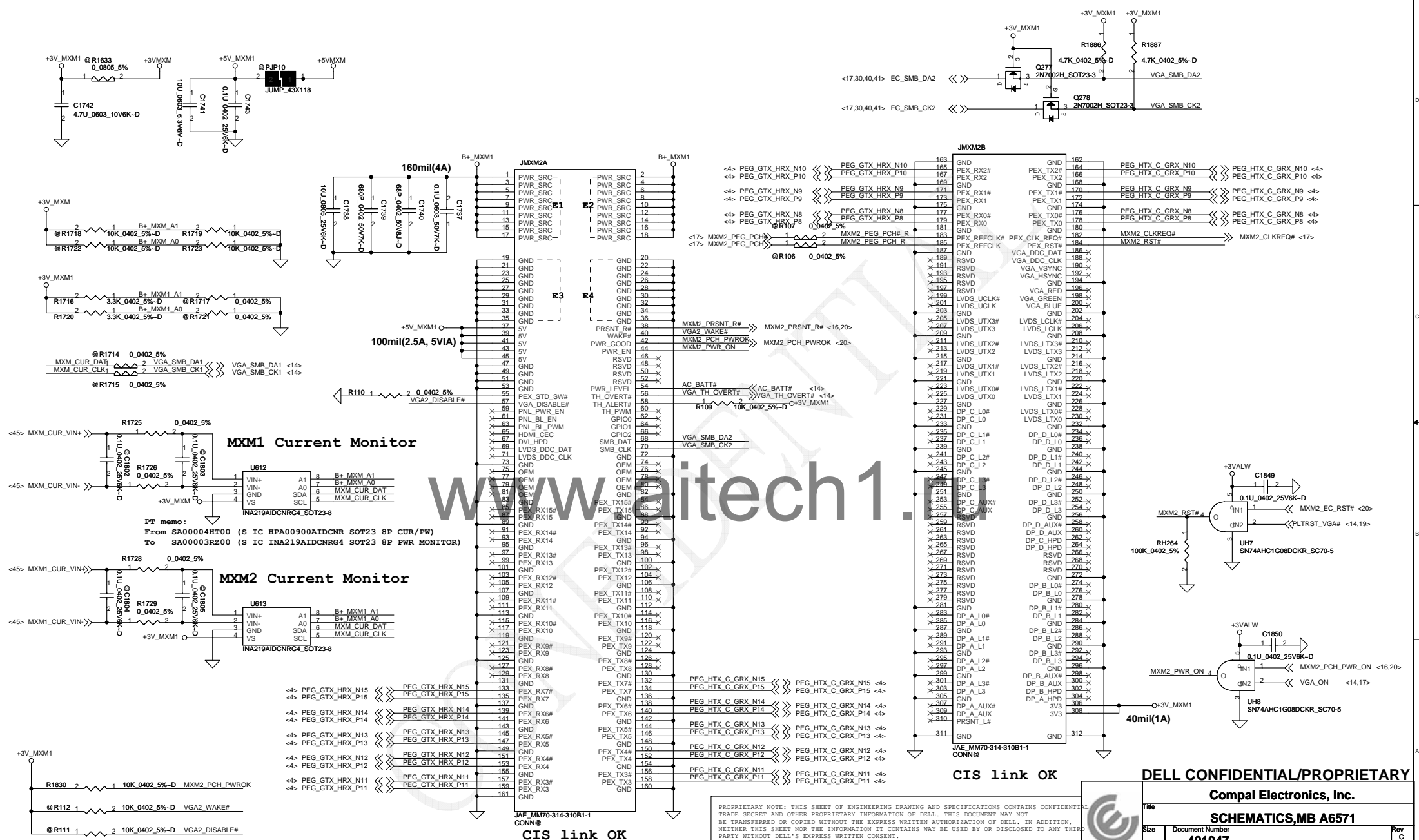
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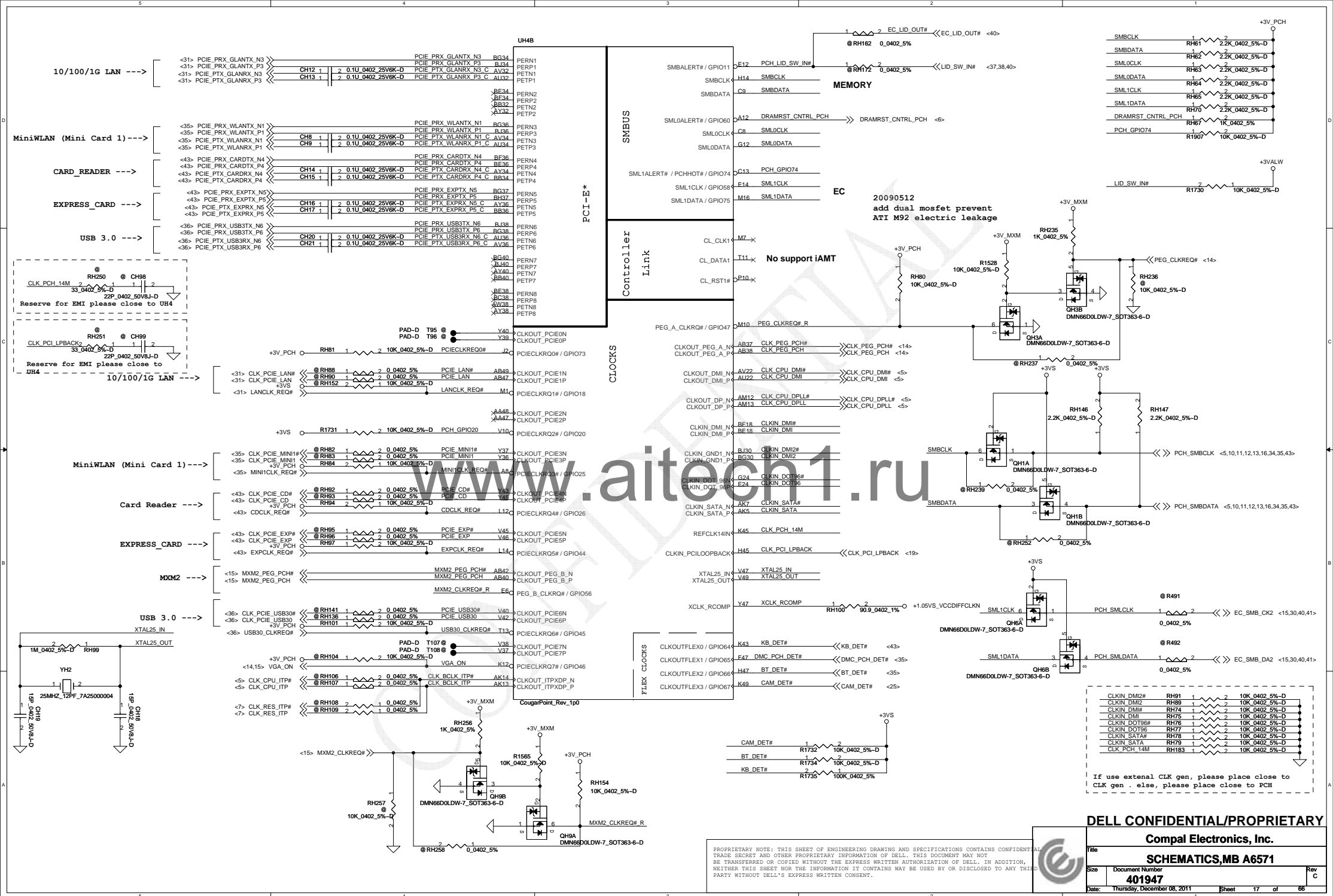
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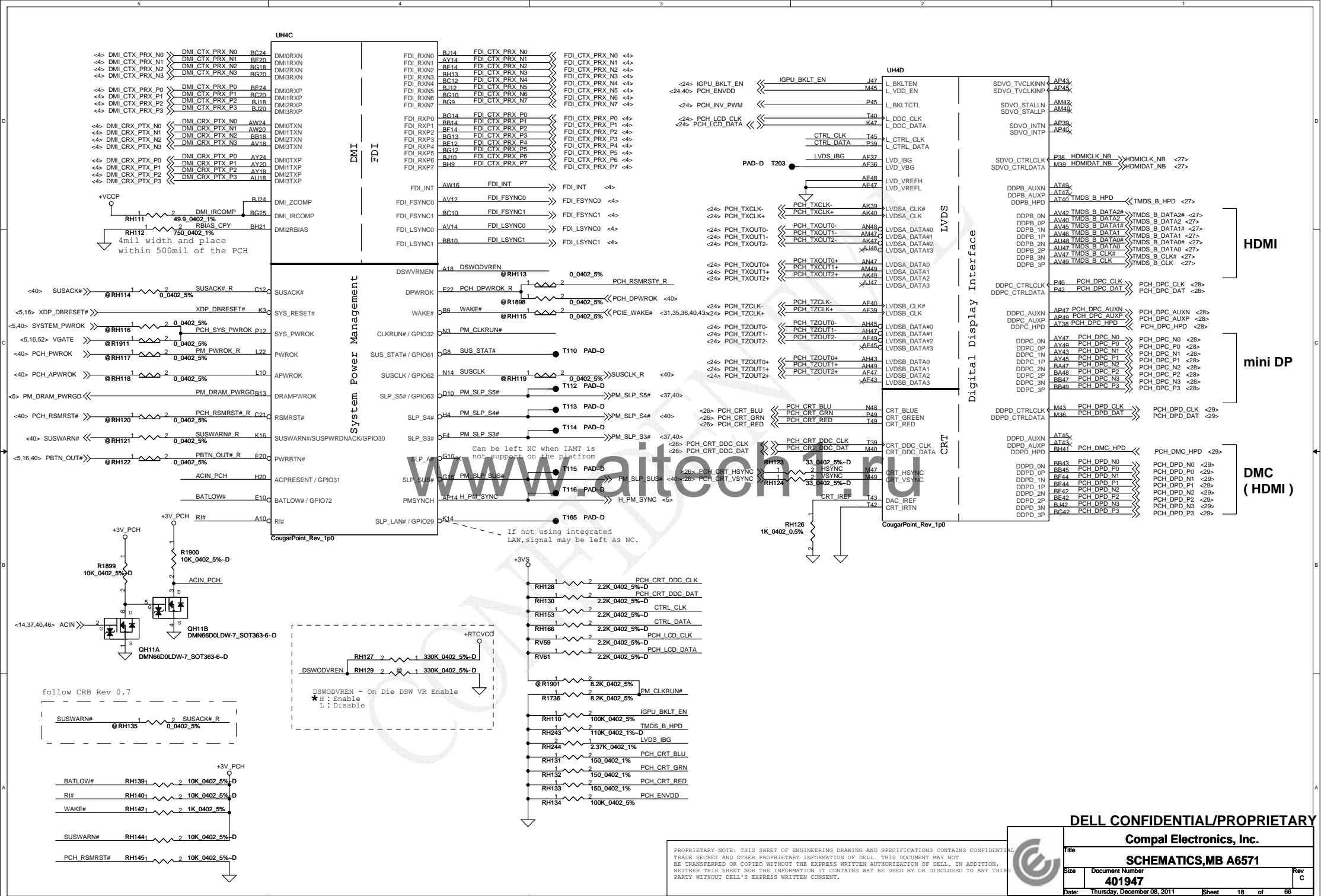


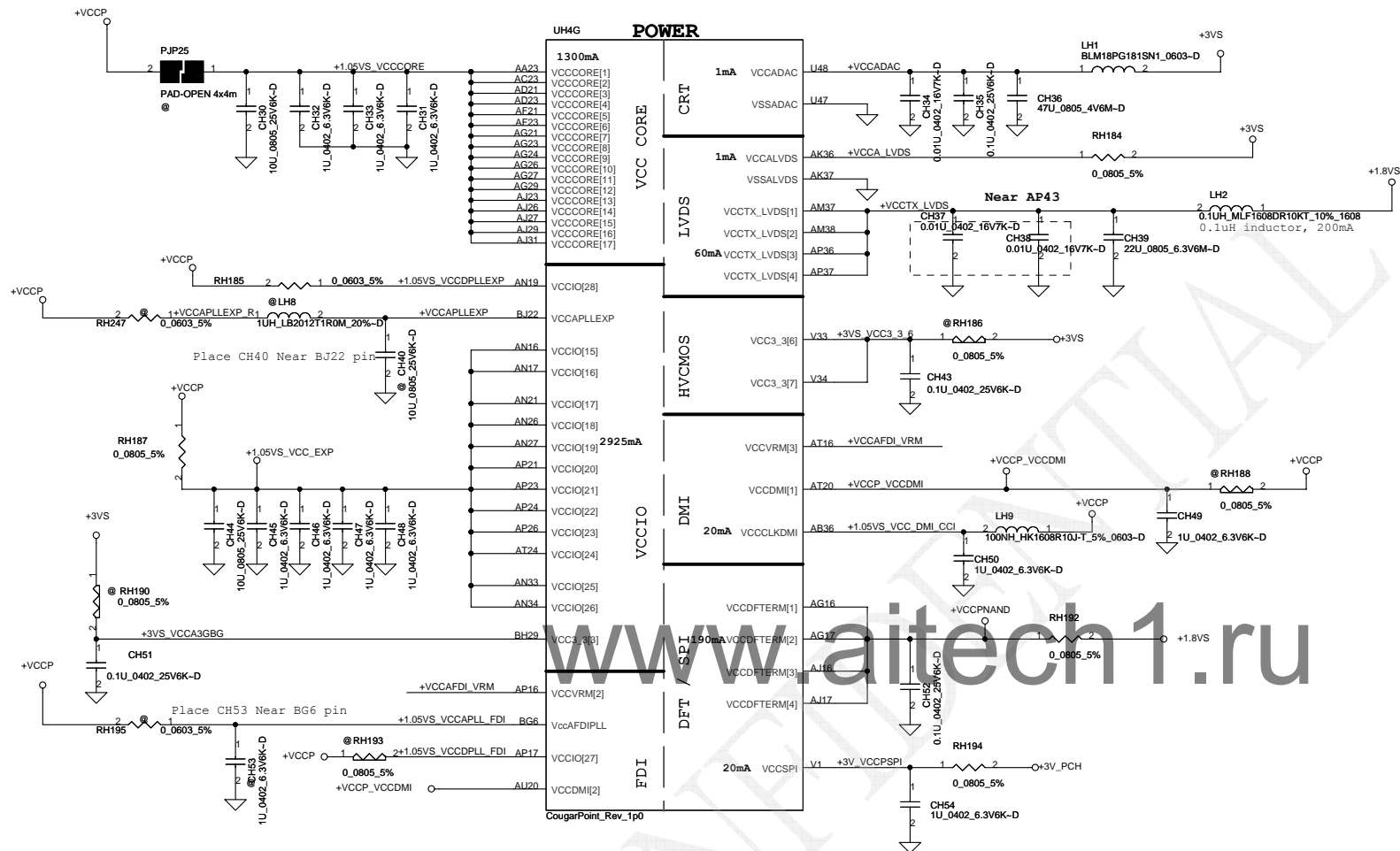


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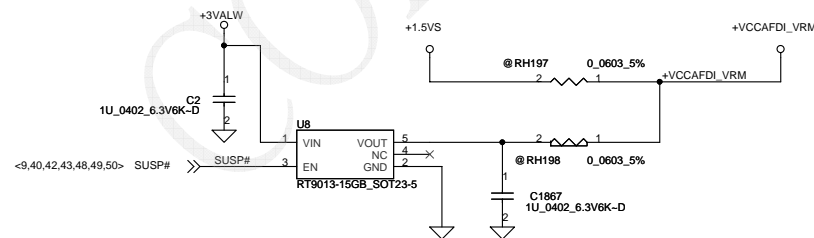






PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLL	1.05	0.08
VccADPLL	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccLVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec

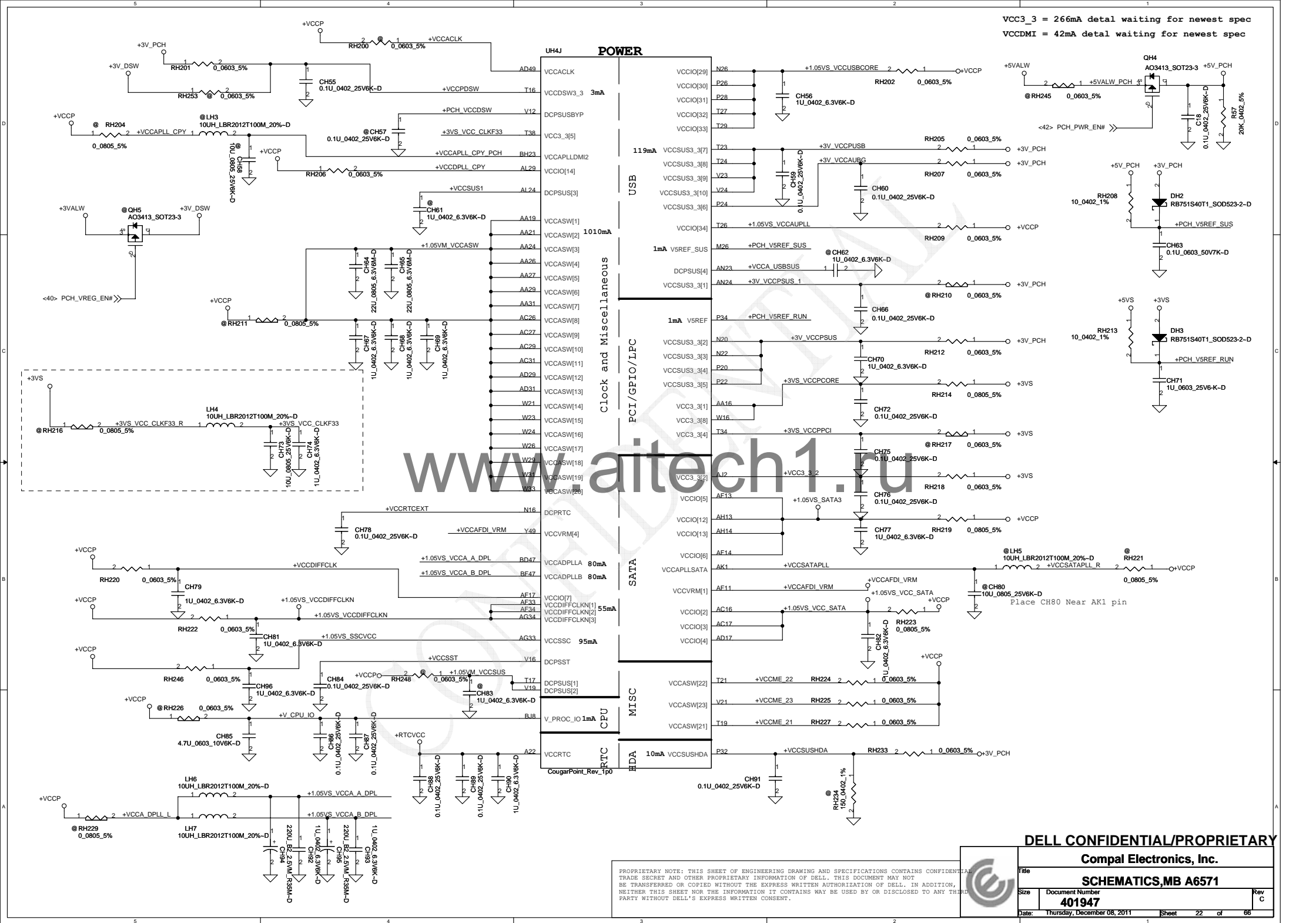


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UH4H	
H5	VSS[0]
AA17	VSS[1]
AA2	VSS[2]
AA3	VSS[3]
AA33	VSS[4]
AA34	VSS[5]
AB11	VSS[6]
AB14	VSS[7]
AB39	VSS[8]
AB4	VSS[9]
AB43	VSS[10]
AB5	VSS[11]
AB7	VSS[12]
AC19	VSS[13]
AC2	VSS[14]
AC21	VSS[15]
AC24	VSS[16]
AC33	VSS[17]
AC34	VSS[18]
AC48	VSS[19]
AD10	VSS[20]
AD11	VSS[21]
AD12	VSS[22]
AD13	VSS[23]
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AD27	VSS[27]
AD33	VSS[28]
AD34	VSS[29]
AD36	VSS[30]
AD37	VSS[31]
AD38	VSS[32]
AD39	VSS[33]
AD4	VSS[34]
AD40	VSS[35]
AD42	VSS[36]
AD43	VSS[37]
AD45	VSS[38]
AD46	VSS[39]
AD8	VSS[40]
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AE3	VSS[42]
AF10	VSS[43]
AF12	VSS[44]
AD14	VSS[45]
AD16	VSS[46]
AF16	VSS[47]
AF19	VSS[48]
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AG2	VSS[62]
AG31	VSS[63]
AG48	VSS[64]
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AH3	VSS[66]
AH36	VSS[67]
AH39	VSS[68]
AH40	VSS[69]
AH42	VSS[70]
AH46	VSS[71]
AH7	VSS[72]
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AJ21	VSS[74]
AJ24	VSS[75]
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AK3	VSS[79]
CougarPoint_Rev_1p0	

UH4I	
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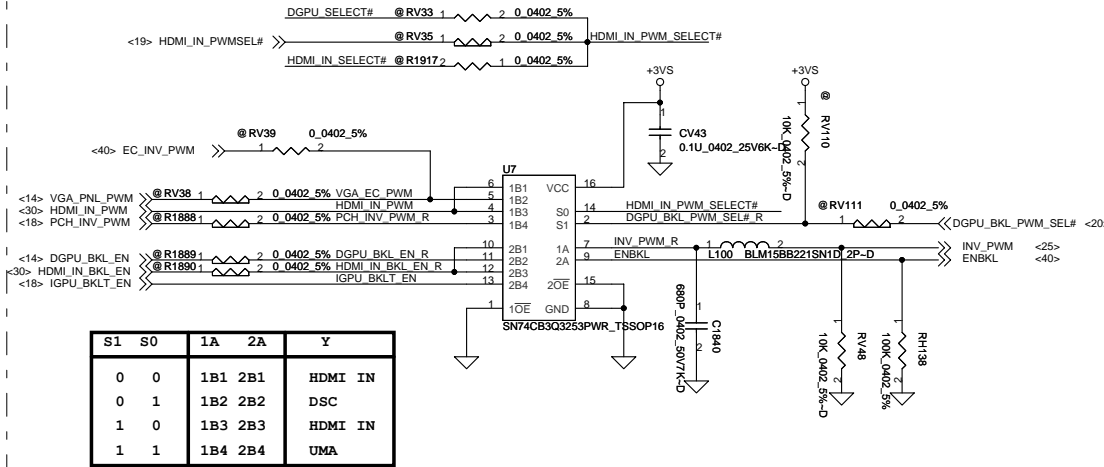
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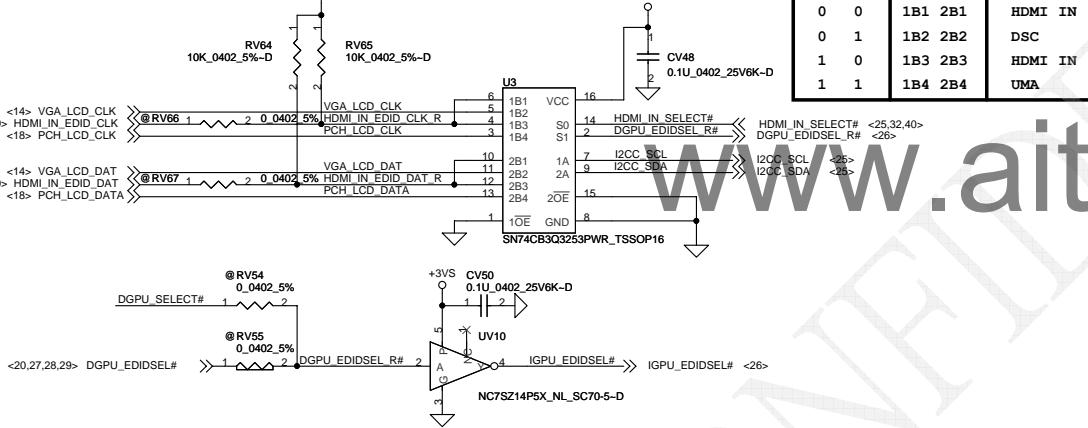
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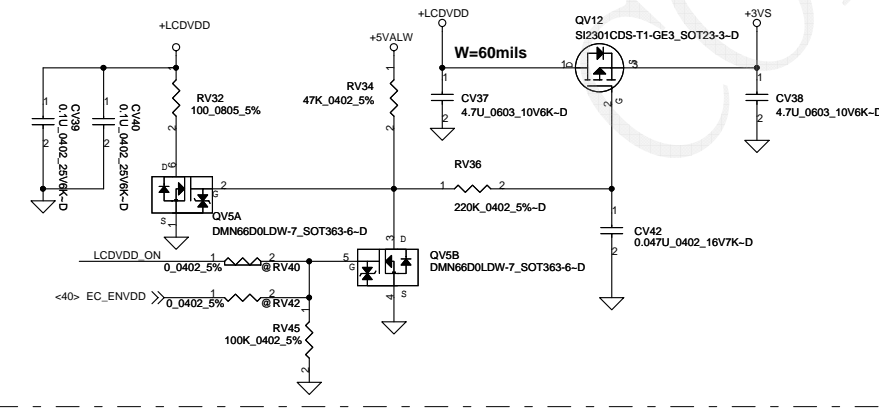
LCD Backlight / PWM Selector



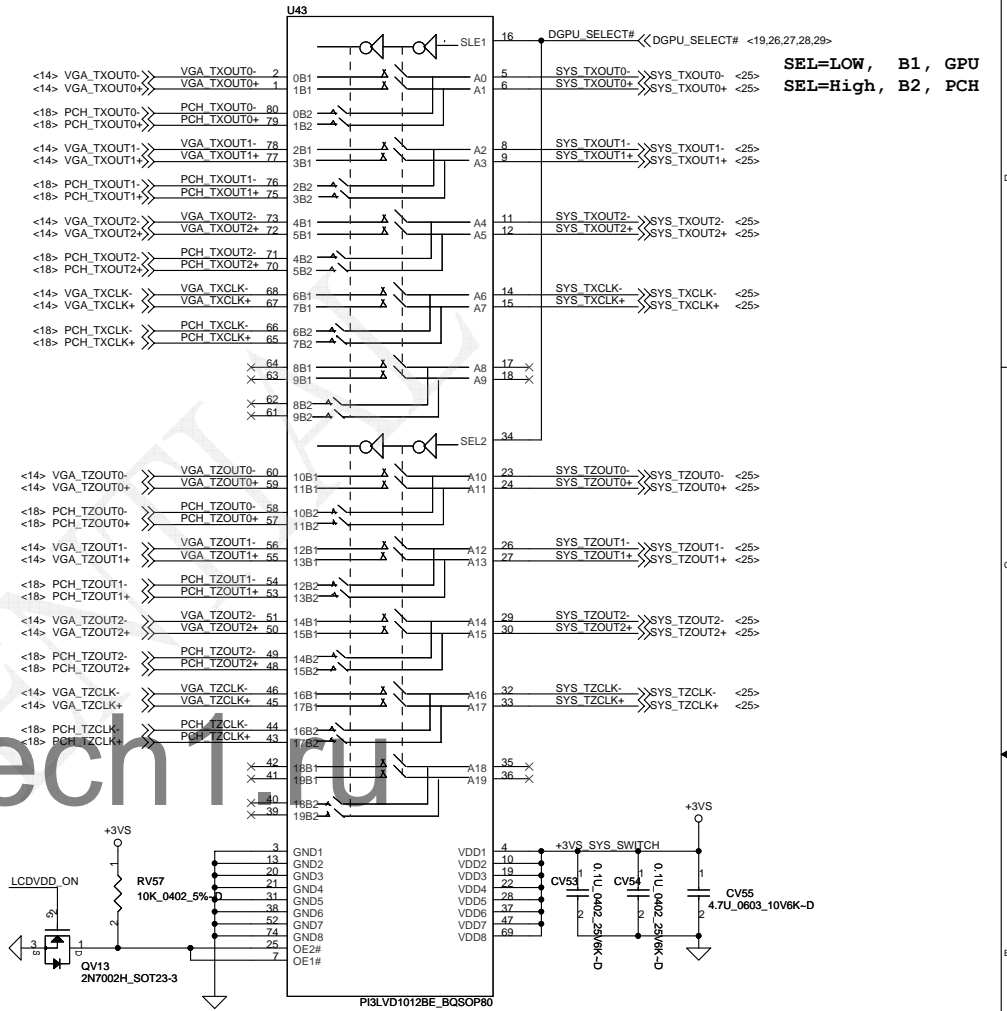
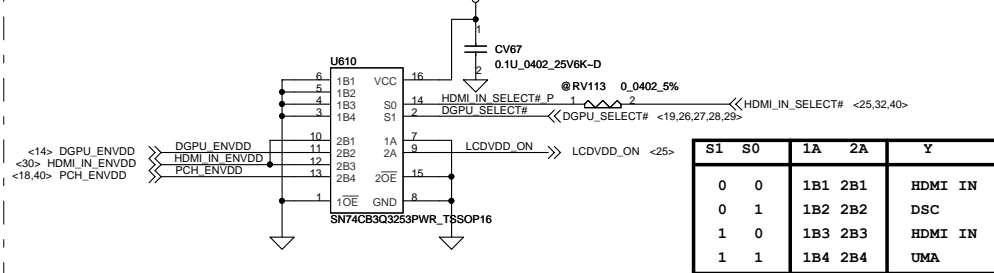
LCD DDC Selector



LCD POWER



LCD VDD Selector



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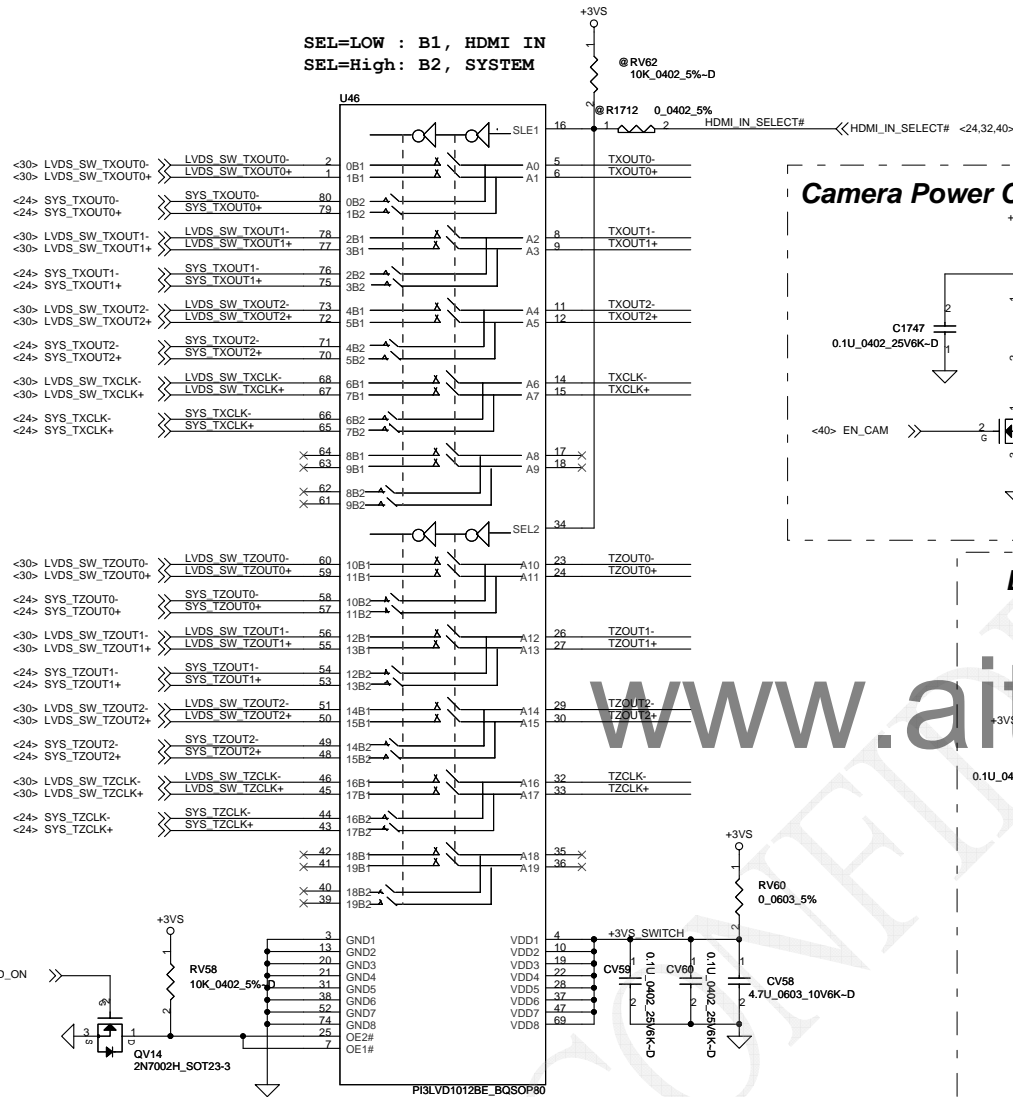
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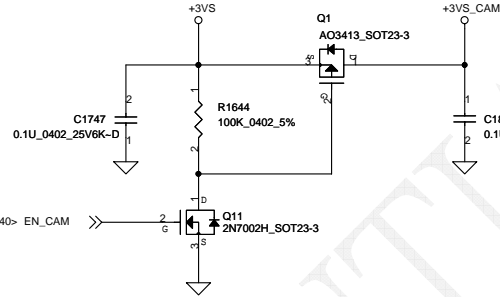
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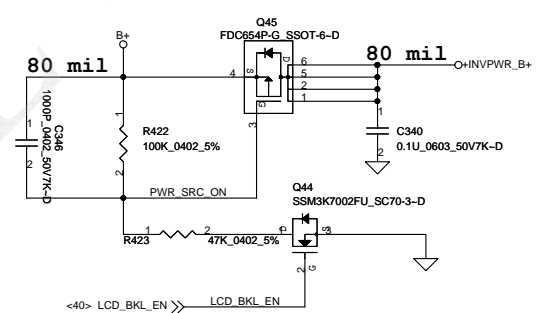
SEL=LOW : B1, HDMI IN
SEL=High: B2, SYSTEM



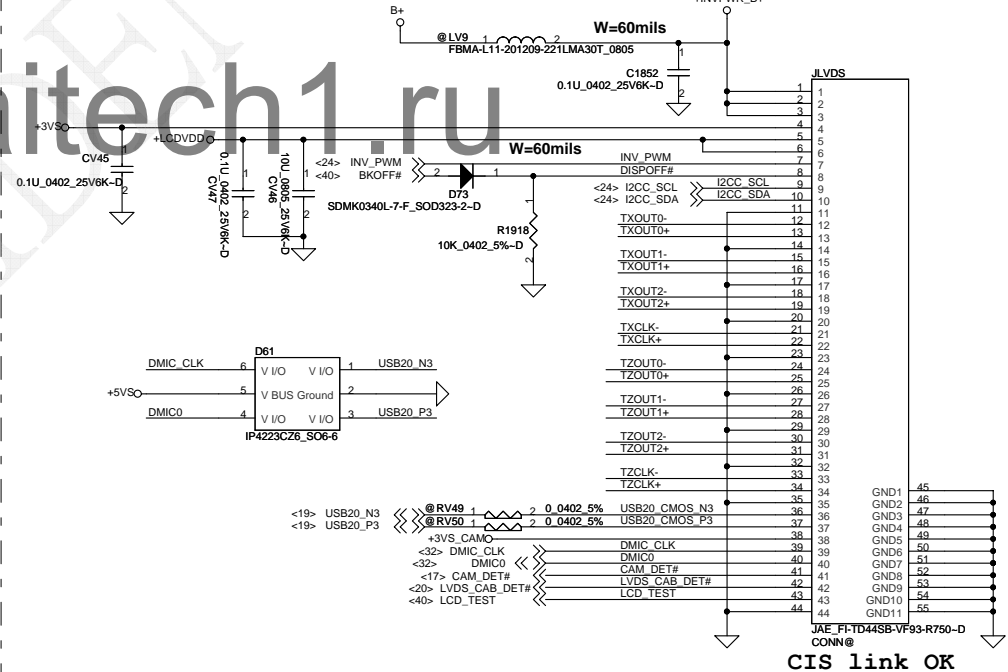
Camera Power Control



LCD Backlight Control



LVDS Connector



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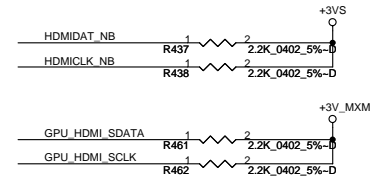
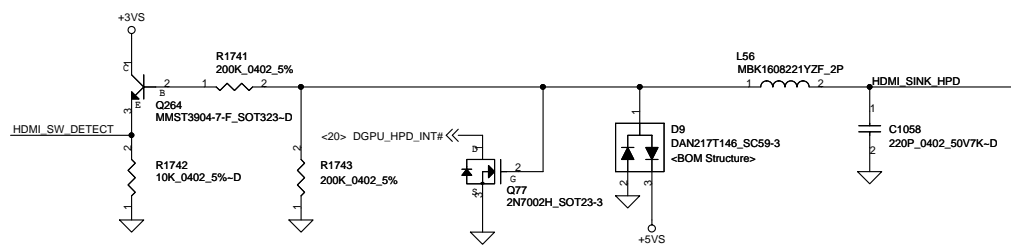
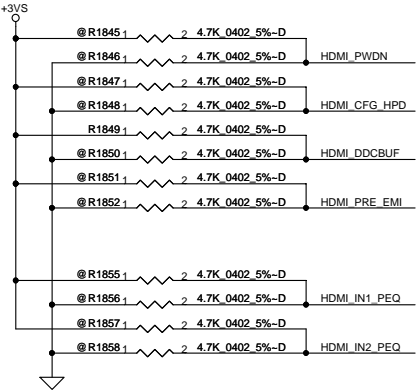
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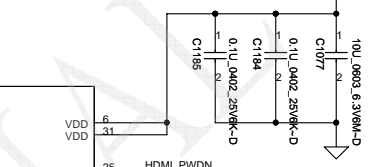
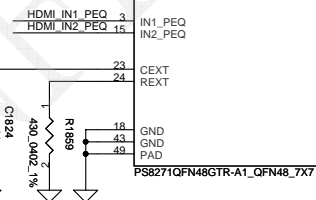
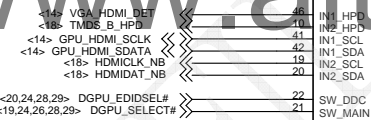
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<14>	GPU_HDMI_TXD2-	C1059	2	1	0.1U_0402_25V6K-D	GPU_HDMI_C_TX2-	44	IN1_D1n
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<14>	GPU_HDMI_TXD1-	C1061	2	1	0.1U_0402_25V6K-D	GPU_HDMI_C_TX1-	47	IN1_D2n
<14>	GPU_HDMI_TXD1+	C1062	2	1	0.1U_0402_25V6K-D	GPU_HDMI_C_TX1+	48	IN1_D2p
<14>	GPU_HDMI_TXD0-	C1063	2	1	0.1U_0402_25V6K-D	GPU_HDMI_C_TX0-	2	IN1_D3n
<14>	GPU_HDMI_TXD0+	C1064	2	1	0.1U_0402_25V6K-D	GPU_HDMI_C_TX0+	2	IN1_D3p
<14>	GPU_HDMI_TXC-	C1065	2	1	0.1U_0402_25V6K-D	GPU_HDMI_C_CLK-	4	IN1_D4n
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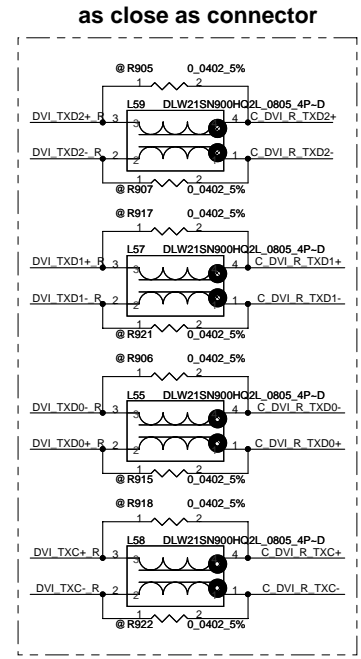
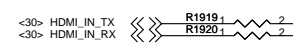
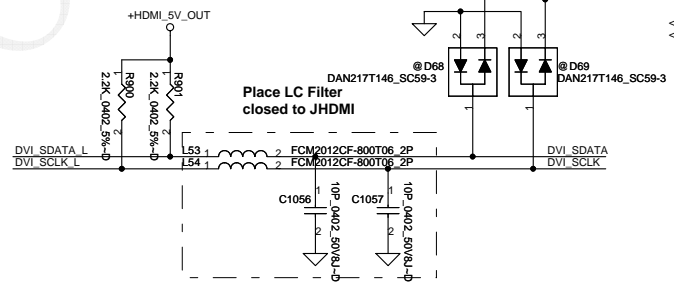
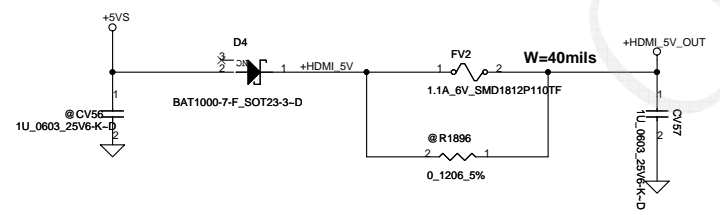
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<18>	TMDS_B_DATA2	TMDS_B_DATA2	C1114	2	1	0.1U_0402_25V6K-D	PCH_HDMI_C_TXD2+	9	IN2_D1p
<18>	TMDS_B_DATA1#	TMDS_B_DATA1#	C1123	2	1	0.1U_0402_25V6K-D	PCH_HDMI_C_TXD1-	11	IN2_D2n
<18>	TMDS_B_DATA1	TMDS_B_DATA1	C1116	2	1	0.1U_0402_25V6K-D	PCH_HDMI_C_TXD1+	12	IN2_D2p
<18>	TMDS_B_DATA0#	TMDS_B_DATA0#	C1122	2	1	0.1U_0402_25V6K-D	PCH_HDMI_C_TXD0-	13	IN2_D3n
<18>	TMDS_B_DATA0	TMDS_B_DATA0	C1115	2	1	0.1U_0402_25V6K-D	PCH_HDMI_C_TXD0+	14	IN2_D3p
<18>	TMDS_B_CLK#	TMDS_B_CLK#	C1124	2	1	0.1U_0402_25V6K-D	PCH_HDMI_C_TXC-	16	IN2_D4n
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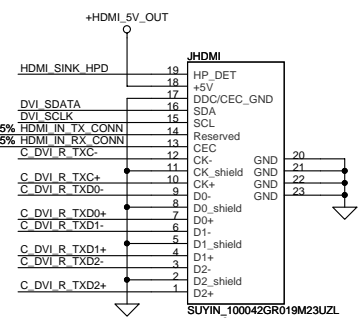
6	VDD	HDMI_PWDN
31	VDD	HDMI_CFG_HPD
25	HDMI_PWDN	
28	HDMI_CFG_HPD	
40	HDMI_DDCBUF	
34	HDMI_PRE_EMI	
7	X	

36	DVI_TXD2- R
35	DVI_TXD2+ R
33	DVI_TXD1- R
32	DVI_TXD1+ R
30	DVI_TXD0- R
29	DVI_TXD0+ R
27	DVI_TXC- R
26	DVI_TXC+ R

SEL	Y
0	IN1
1	IN2



HDMI Connector



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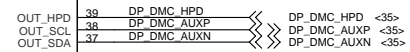
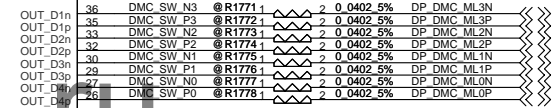
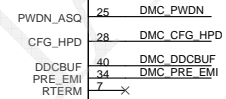
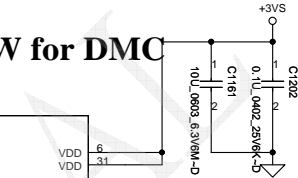
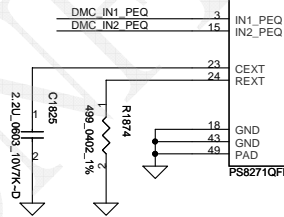
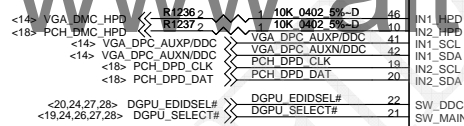
PCH/GPU AUX&LANE SW for DMC



<14> VGA_DPC_P3	C1110	2	0.1U	0402	25V6K-D	VGA DPC SW N3	44	INT_D1n
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<14> VGA_DPC_P2	C1111	1	0.1U	0402	25V6K-D	VGA DPC SW N2	47	INT_D2n
<14> VGA_DPC_N2	C1083	2	0.1U	0402	25V6K-D	VGA DPC SW P2	48	INT_D2p
<14> VGA_DPC_N1	C1112	1	0.1U	0402	25V6K-D	VGA DPC SW N1	1	INT_D3n
<14> VGA_DPC_P1	C1085	1	0.1U	0402	25V6K-D	VGA DPC SW P1	2	INT_D3p
<14> VGA_DPC_N0	C1084	2	0.1U	0402	25V6K-D	VGA DPC SW N0	4	INT_D4n
<14> VGA_DPC_P0	C1082	2	0.1U	0402	25V6K-D	VGA DPC SW P0	5	INT_D4p

From Intel PCH

<18> PCH DPD_P3	C1149	1	2	0.1U	0402	25VK-0	PCH DPD SW N3	8	In2_D1n
<18> PCH DPD_N3	C1148	1	2	0.1U	0402	25VK-0	PCH DPD SW P3	9	In2_D1n
<18> PCH DPD_P2	C1147	1	2	0.1U	0402	25VK-0	PCH DPD SW N2	11	In2_D2n
<18> PCH DPD_P2	C1146	1	2	0.1U	0402	25VK-0	PCH DPD SW P2	12	In2_D2n
<18> PCH DPD_N1	C1145	1	2	0.1U	0402	25VK-0	PCH DPD SW N1	13	In2_D3n
<18> PCH DPD_P1	C1144	1	2	0.1U	0402	25VK-0	PCH DPD SW P1	14	In2_D3n
<18> PCH DPD_P0	C1143	1	2	0.1U	0402	25VK-0	PCH DPD SW N0	16	In2_D4n
<18> PCH DPD_P0	C1142	1	2	0.1U	0402	25VK-0	PCH DPD SW P0	17	In2_D4n



SEL	Y
0	IN1
1	IN2

The diagram illustrates the power and signal connections for the DMC and PCH components. The main power supply is +3V_MXM, which is connected to a common rail. This rail is connected to the following pins and components:

- DMC_PWDN**: Connected to resistor R1860 (2.2K, 0402 5%-D).
- DMC_CFG_HPD**: Connected to resistor R1861 (2.2K, 0402 5%-D).
- DMC_DDCBUF**: Connected to resistor R1863 (2.2K, 0402 5%-D).
- DMC_PRE_EMI**: Connected to resistor R1867 (2.2K, 0402 5%-D).
- DMC_IN1_PEQ**: Connected to resistor R1870 (2.2K, 0402 5%-D).
- DMC_IN2_PEQ**: Connected to resistor R1873 (2.2K, 0402 5%-D).
- PCH_DPD_CLK**: Connected to resistor R446 (2.2K, 0402 5%-D).
- PCH_DPD_DAT**: Connected to resistor R447 (2.2K, 0402 5%-D).

The common rail is also connected to ground (indicated by a triangle symbol) and to the +3V_MXM supply. The resistors are labeled with their values and part numbers: R1860, R1861, R1863, R1864, R1865, R1866, R1867, R1870, R1871, R1872, R1873, R446, and R447.

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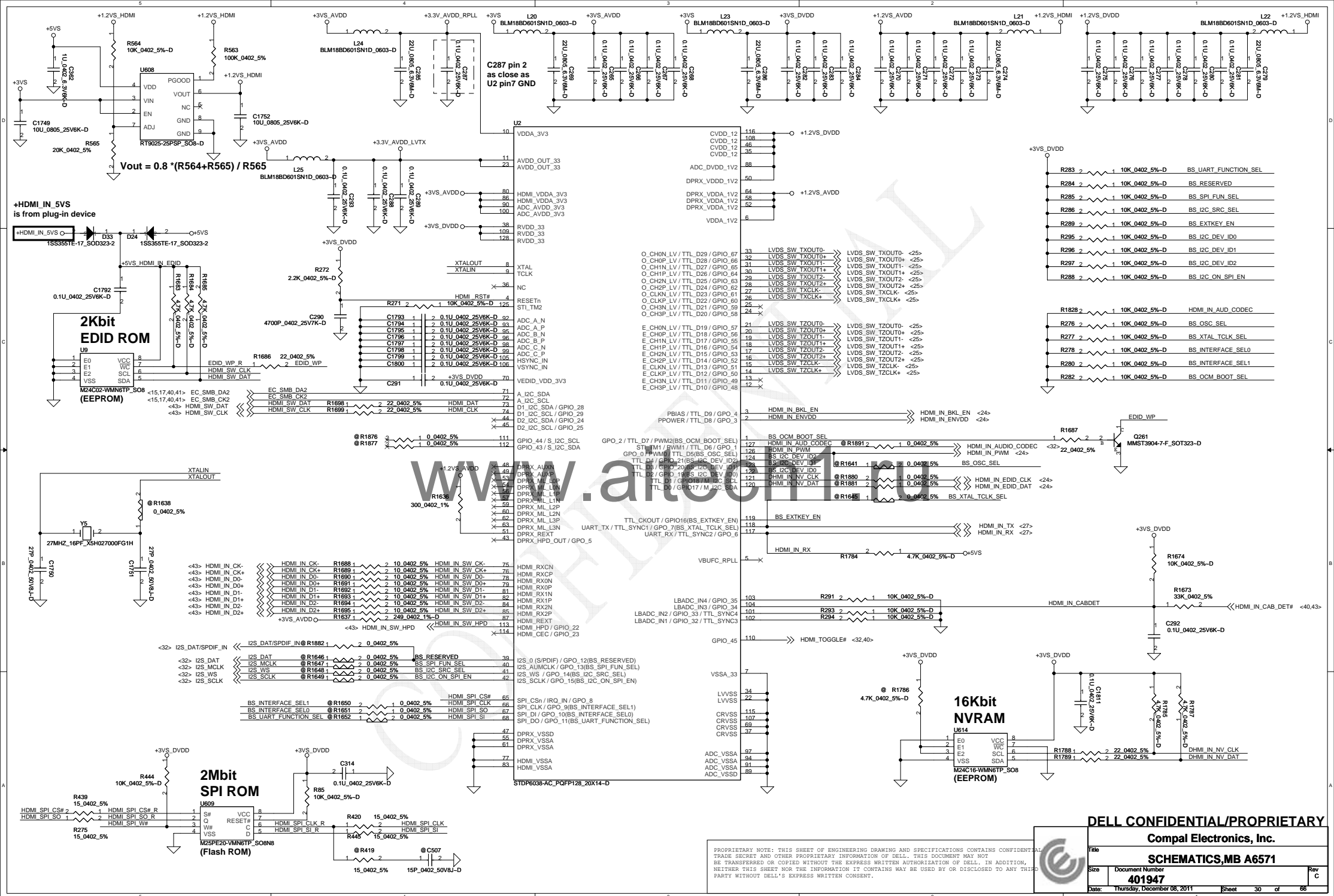
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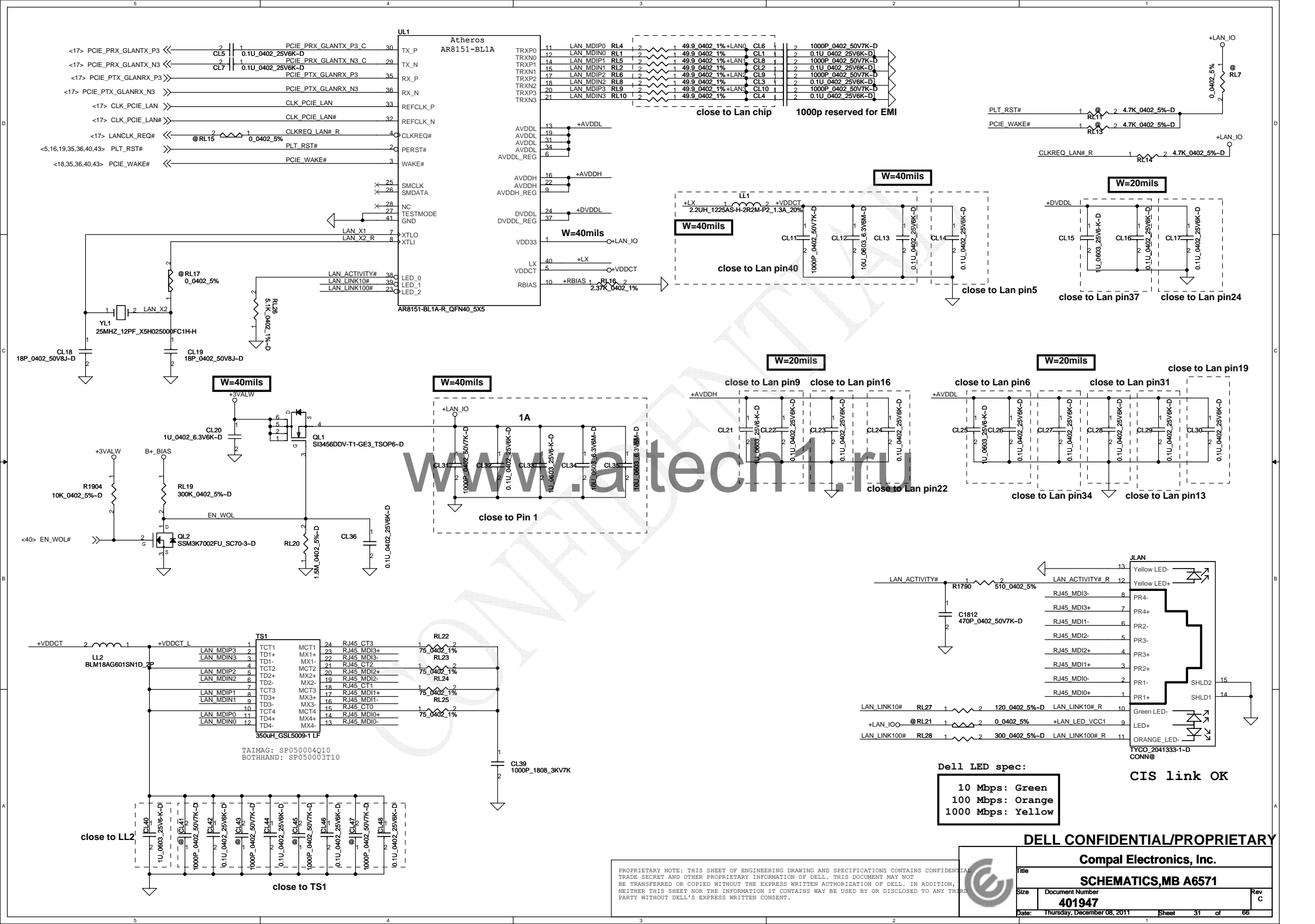
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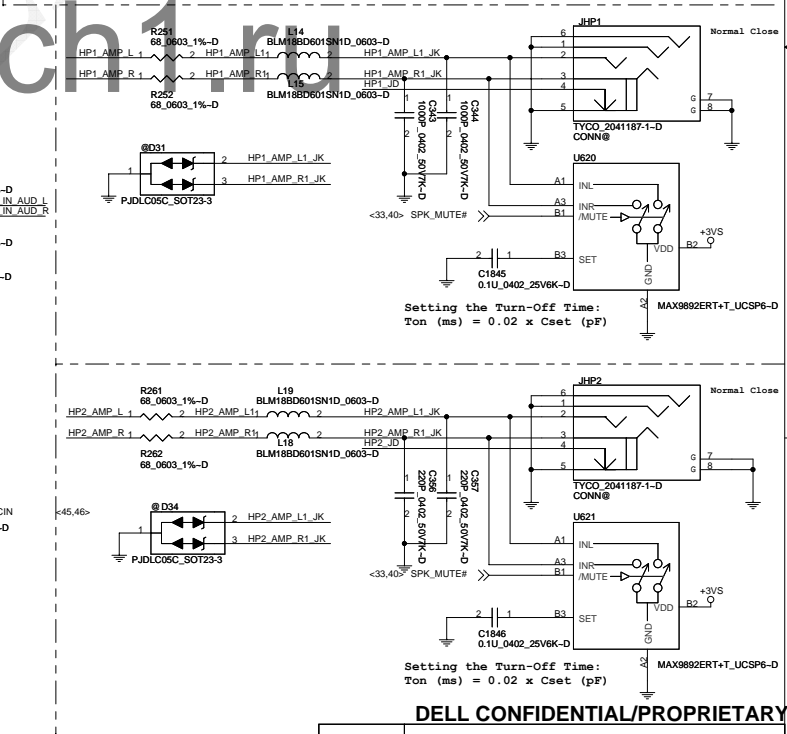
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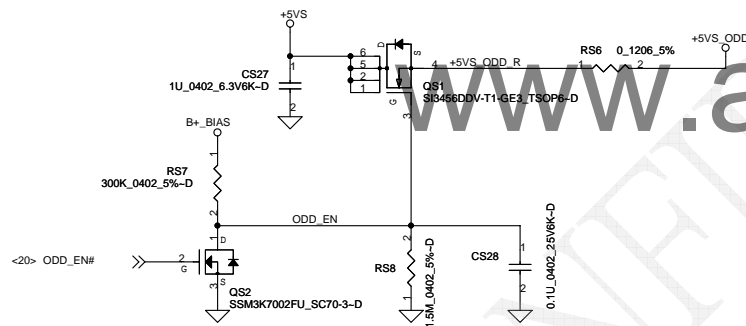
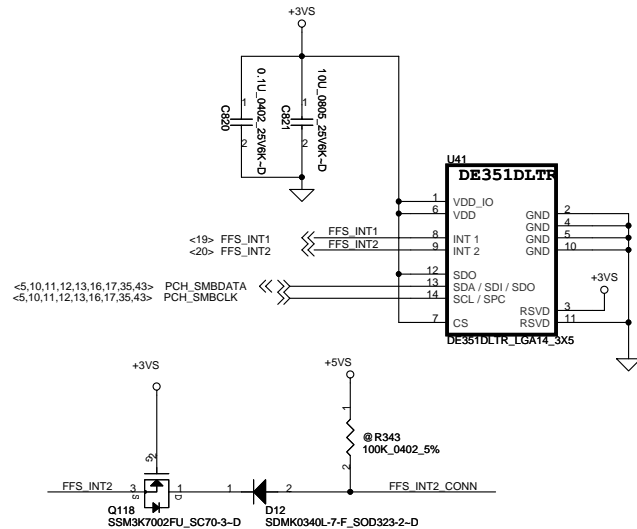
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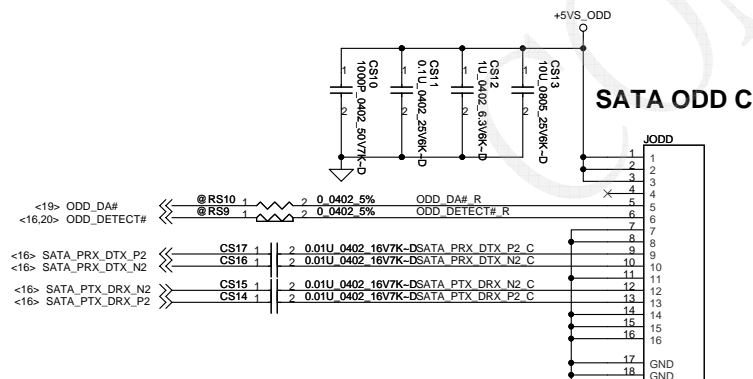


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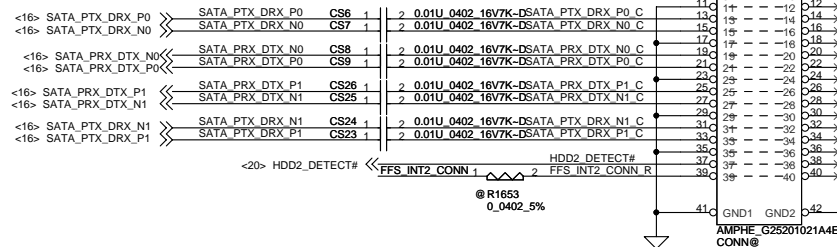
Free Fall Sensor



SATA ODD Conn.



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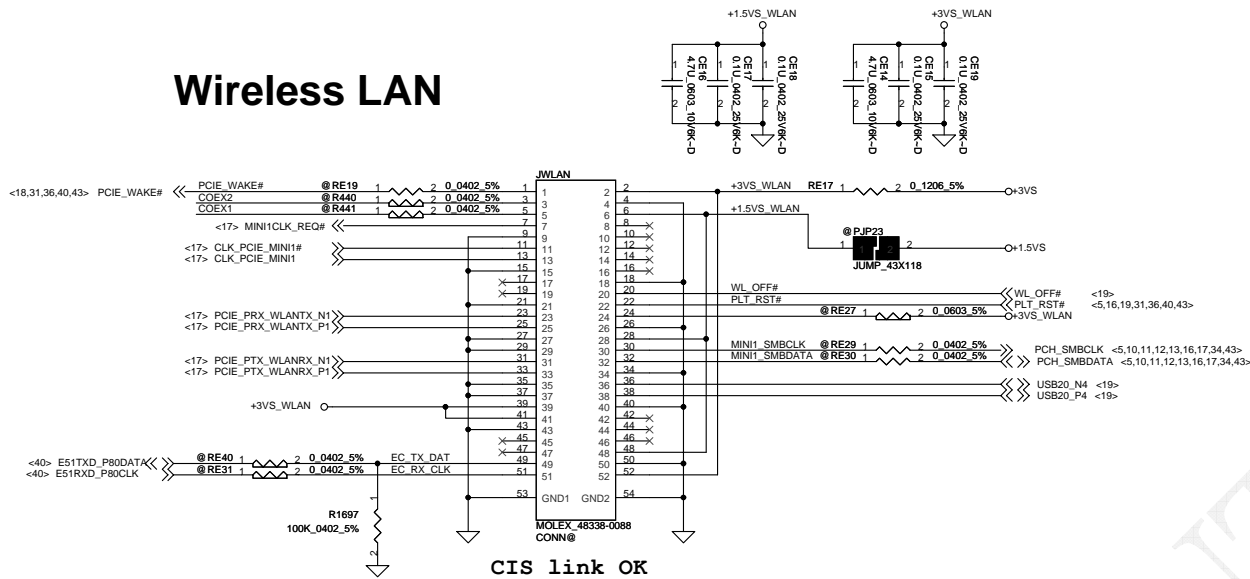
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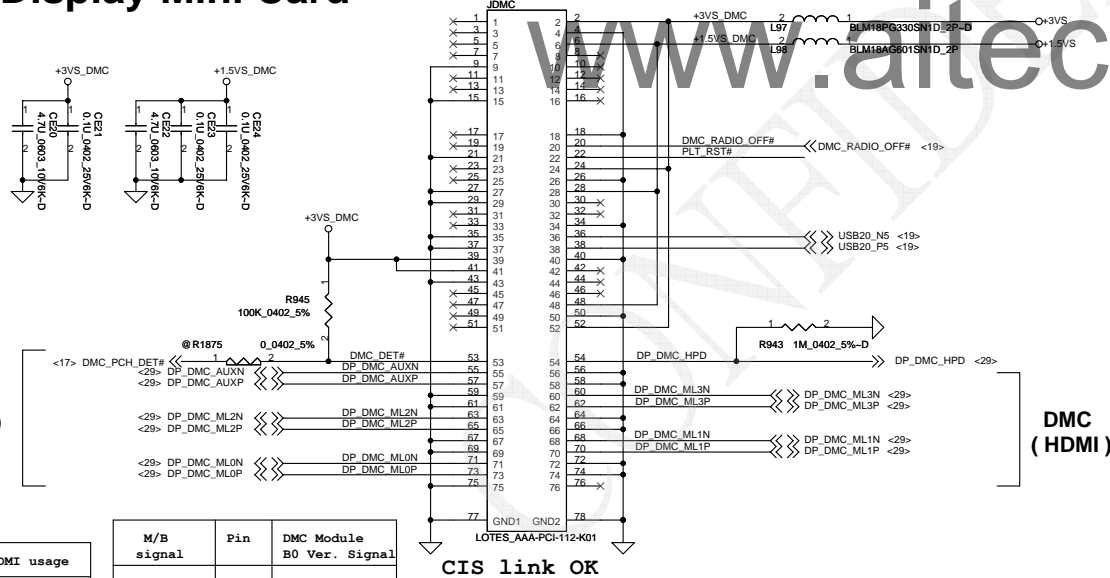
Thursday, December 08, 2011 Sheet 34 of 66

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Wireless LAN

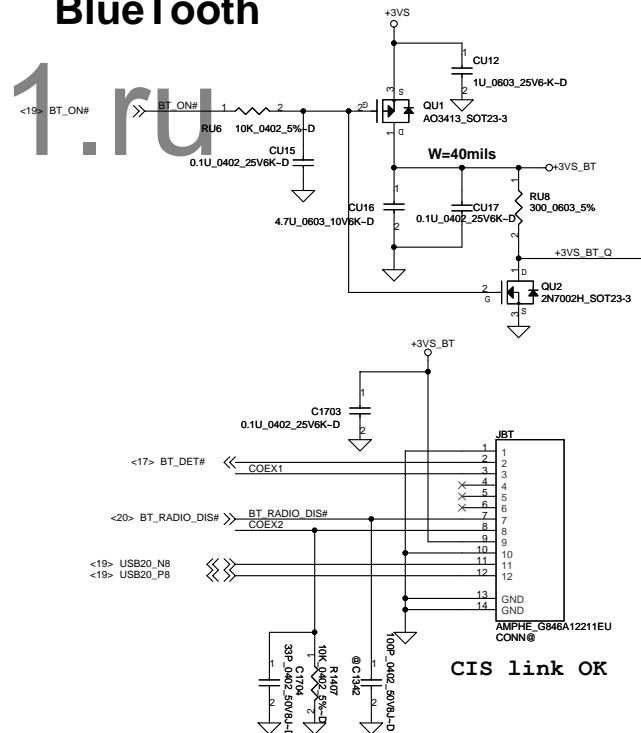


Display Mini Card



PCH DP Port		HDMI usage	M/B signal	Pin	DMC Module B0 Ver. Signal
DDP 0P	TMDS DATA 2		DP_DMC_ML3N	60	DMC_CKN
DDP 0N	TMDS DATA 2#		DP_DMC_ML3P	62	DMC_CKP
DDP 1P	TMDS DATA 1		DP_DMC_ML2N	63	DMC_DON
DDP 1N	TMDS DATA 1#		DP_DMC_ML2P	65	DMC_DOP
DDP 2P	TMDS DATA 0		DP_DMC_ML1N	68	DMC_D1N
DDP 2N	TMDS DATA 0#		DP_DMC_ML1P	70	DMC_D1P
DDP 3P	TMDS CLK		DP_DMC_ML0N	71	DMC_D2N
DDP 3N	TMDS CLK#		DP_DMC_ML0P	73	DMC_D2P
DDP AUXP	HDMI_CTRL_CLK		DP_DMC_AUXN	55	DMC_DDC_DAT
DDP AUXN	HDMI_CTRL_DAT		DP_DMC_AUXP	57	DMC_DDC_CLK

BlueTooth



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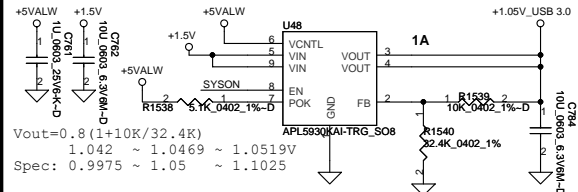
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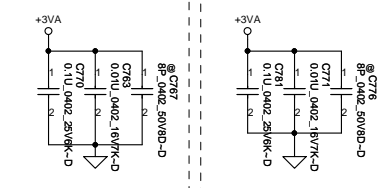
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+1.5V to +1.05V Transfer

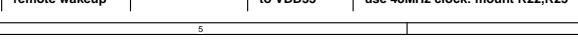
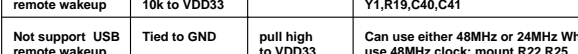
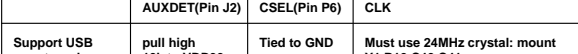
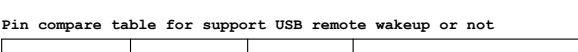
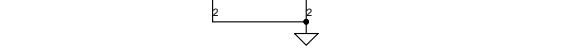
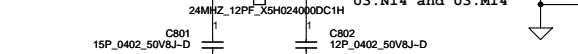
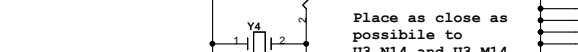
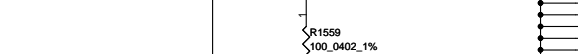
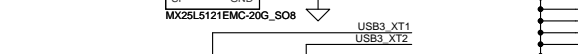
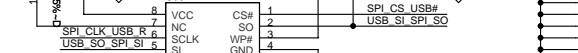
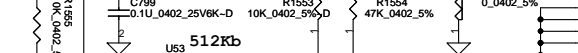
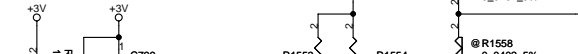
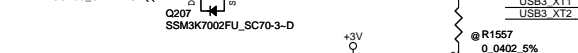
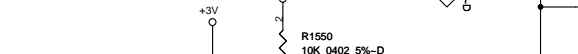
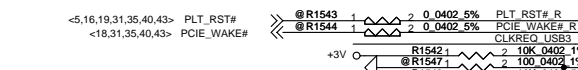
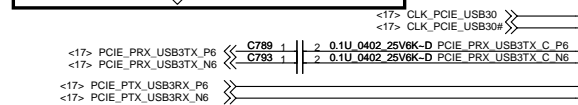
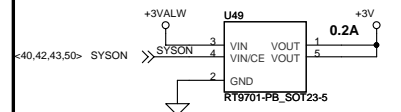


Close to U3.D7

Close to U3.P13



+3VALW to +3V Transfer



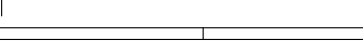
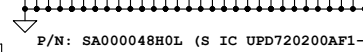
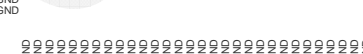
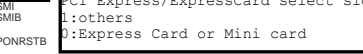
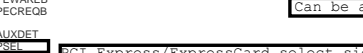
SPEC Max: +3V---200mA; +1.05V---800mA

Idle mode: 0.489W

+3V---43mA; +1.05V---328mA

D3 mode: 0.066W

+3V---5.4mA; +1.05V---45mA



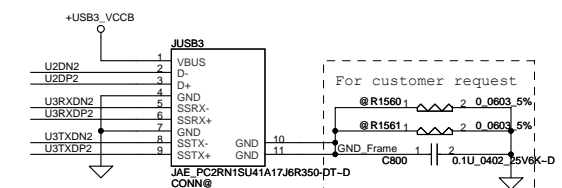
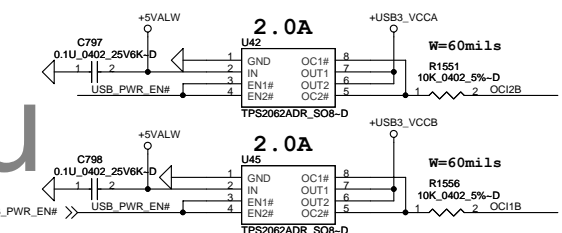
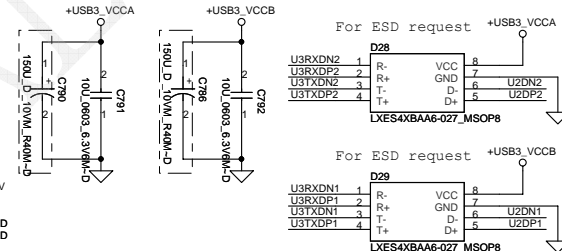
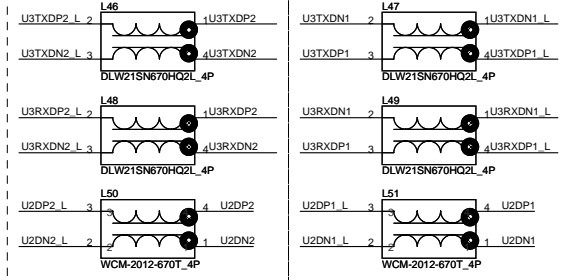
P/N: SA000048H0L (S IC UPD720200AF1-DAP-A FBGA 176P USB3.0)
 A version UPD720200AF1DAPA_FBGA176P-NH-D

Can be attach to EC, either.

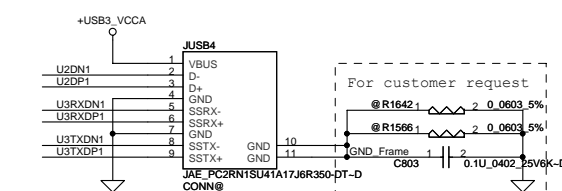
PCI Express/ExpressCard select signal
 1: others
 2: Express Card or Mini card

As short as possible

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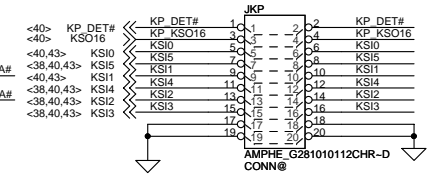
SCHEMATICS_MB A6571

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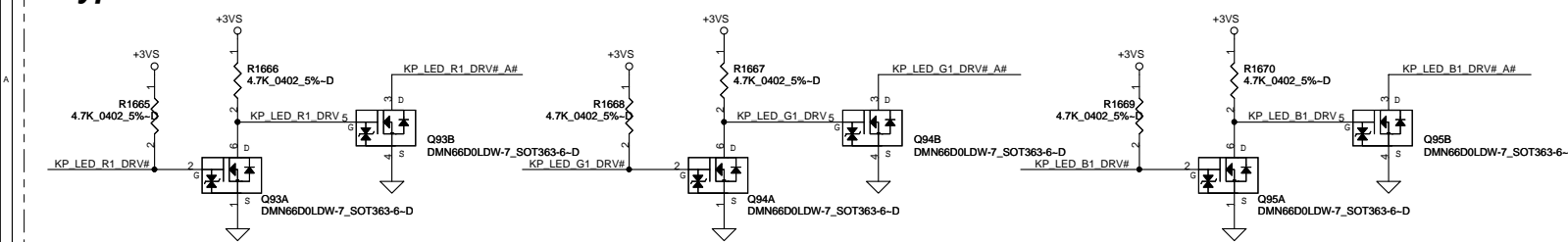
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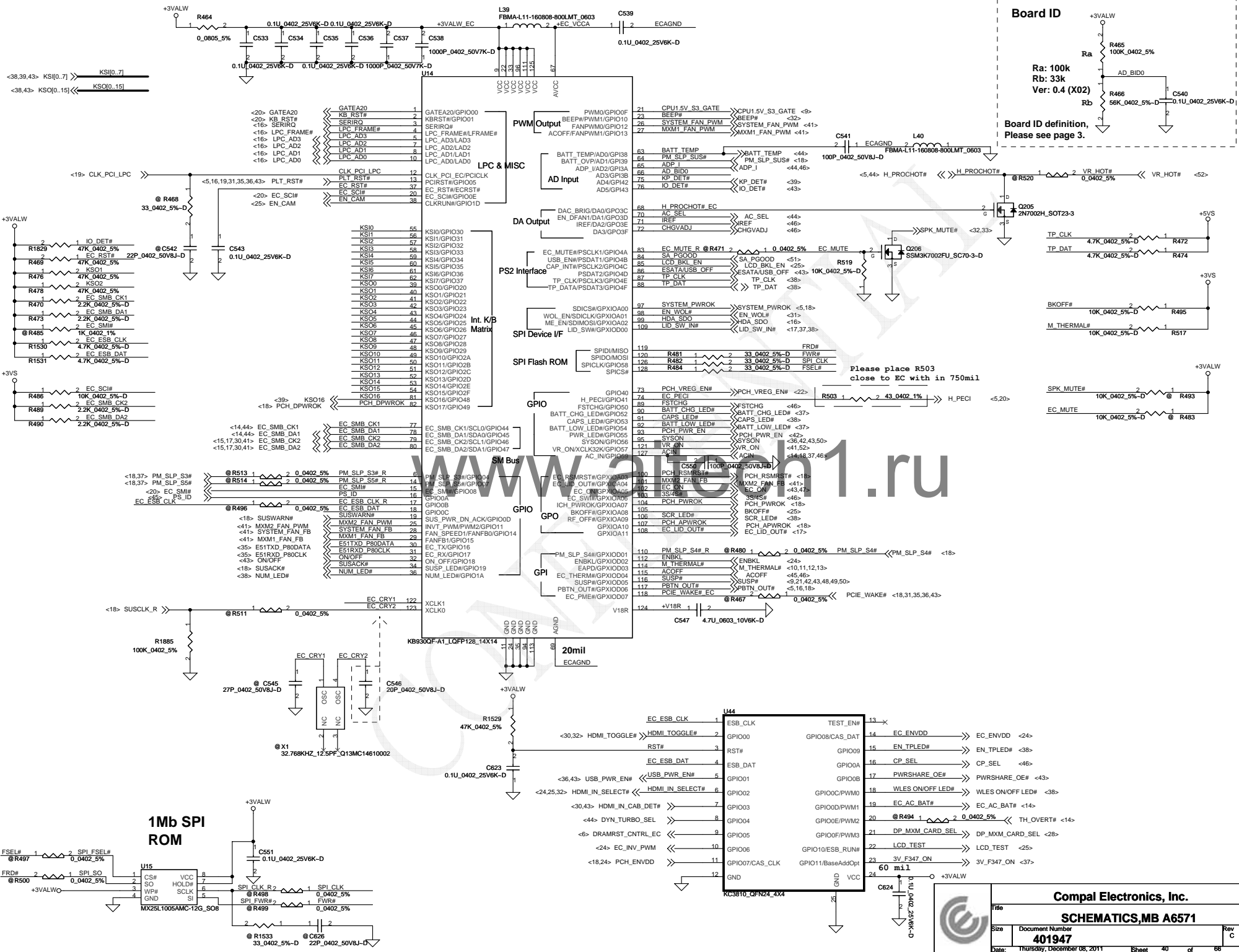
Keypad CONN



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Board ID

Ra: 100k
Rb: 33k
Ver: 0.4 (X02)

Board ID definition, Please see page 3.

Board ID definition, Please see page 3.

TP_CLK 4.7K_0402_5%-D R472
TP_DAT 4.7K_0402_5%-D R474
BKOFF# 10K_0402_5%-D R495
M_THERMAL# 10K_0402_5%-D R517
SPK_MUTE# 10K_0402_5%-D R493
EC_MUTE 10K_0402_5%-D R483

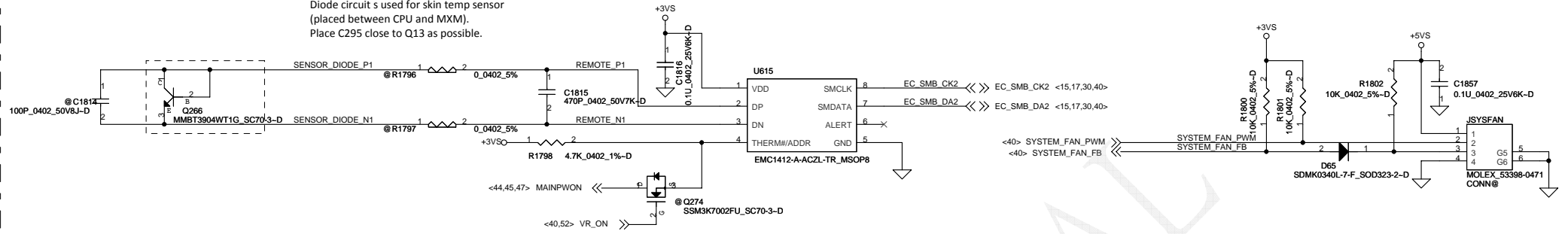
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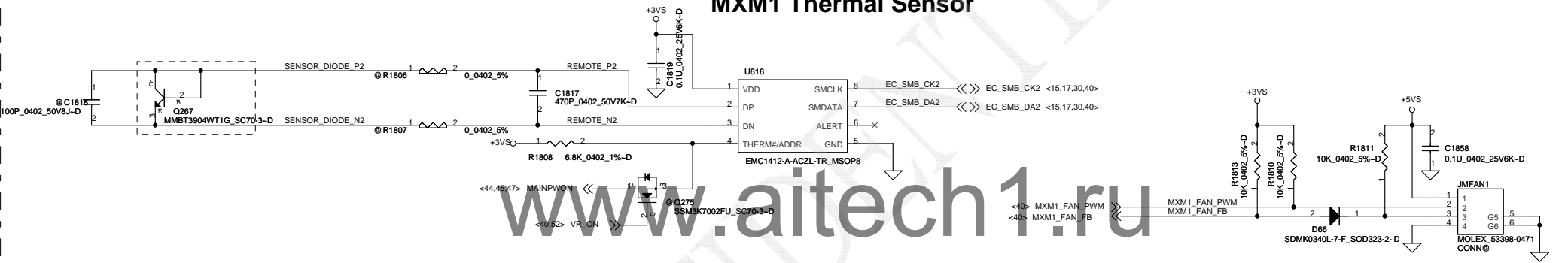
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Size: 401947
Date: Thursday, December 08, 2011
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System Thermal Sensor

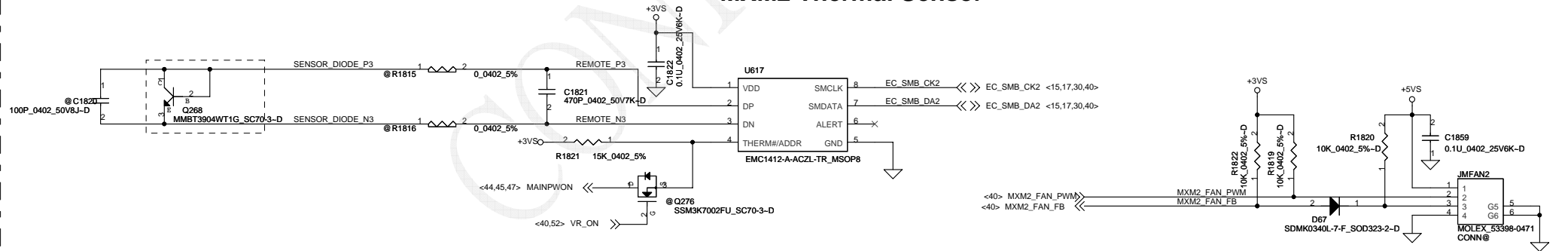
Diode circuit s used for skin temp sensor
(placed between CPU and MXM).
Place C295 close to Q13 as possible.



MXM1 Thermal Sensor



MXM2 Thermal Sensor



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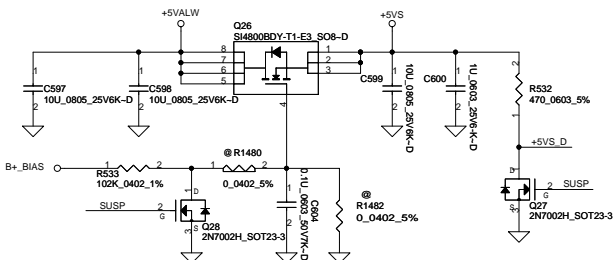
Compal Electronics, Inc.

Title **SCHEMATICS,MB A6571**

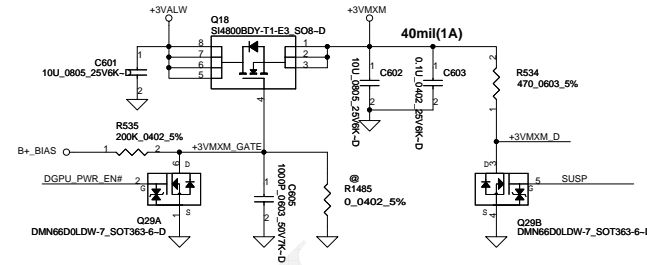
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Date:	Thursday, December 08, 2011	Sheet 41 of 66

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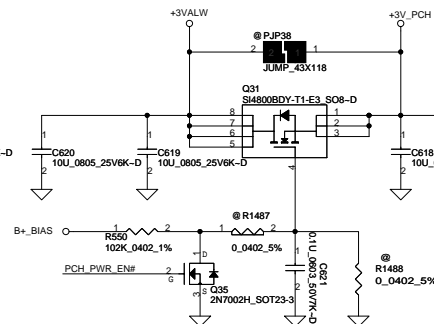
+5VALW to +5VS



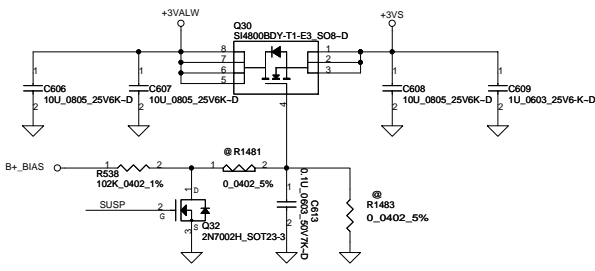
+3VALW to +3VMXM Transfer



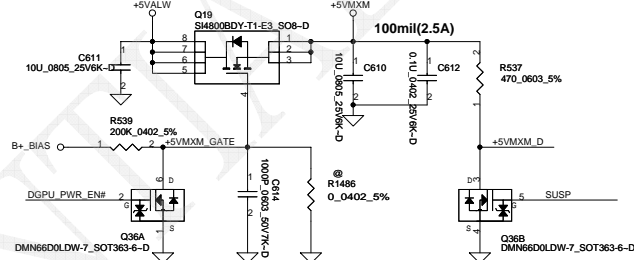
+3VALW to +3V_PCH



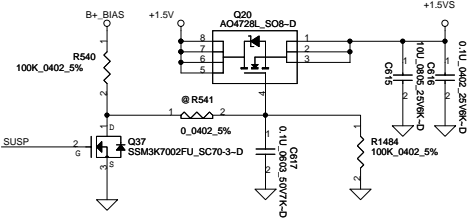
+3VALW to +3VS



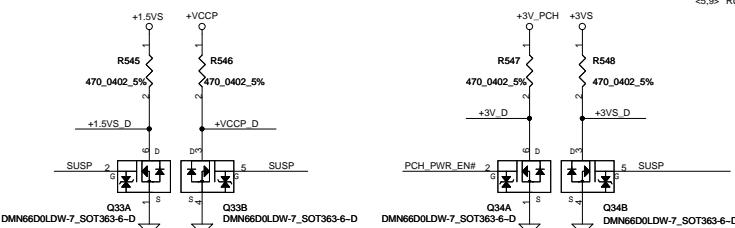
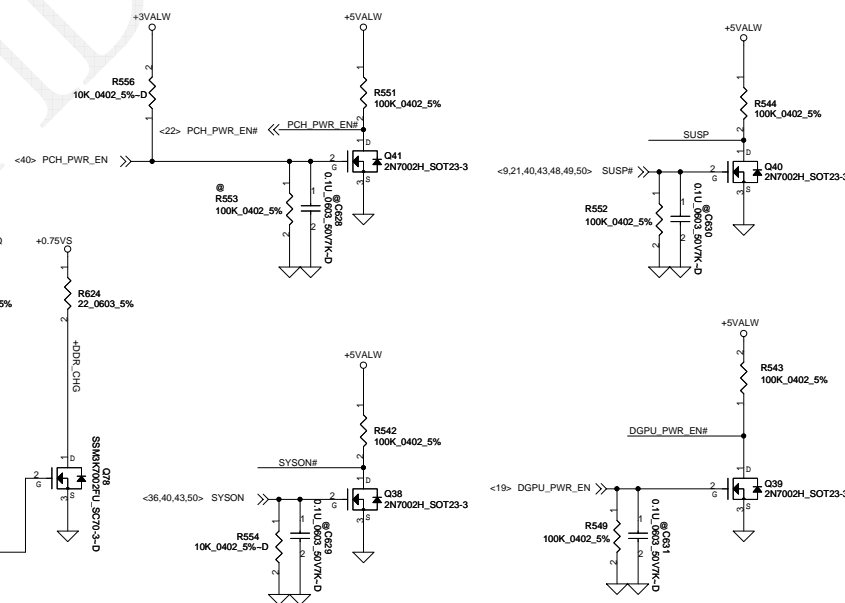
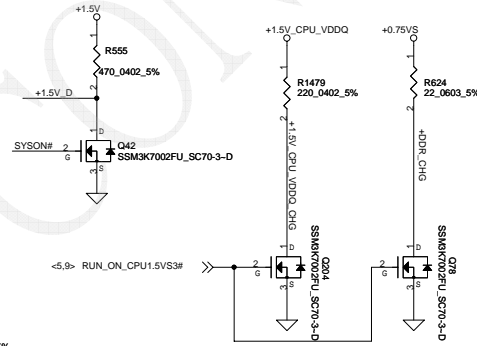
+5VALW to +5VMXM Transfer



+1.5V To +1.5VS



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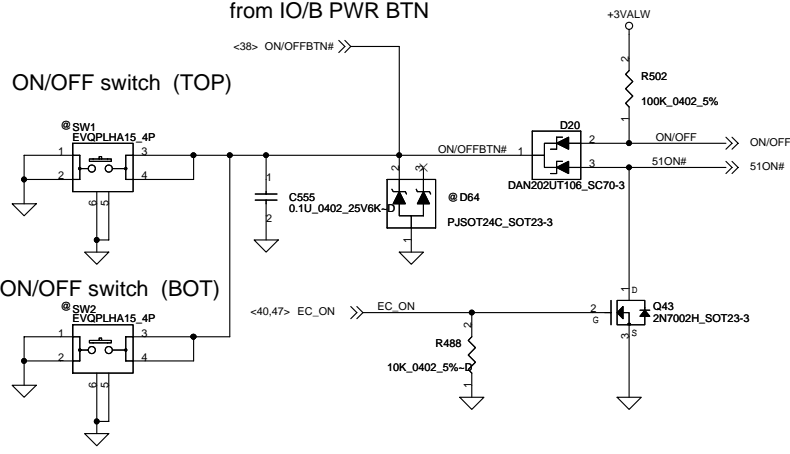
Date: Thursday, December 06, 2011 Sheet 42 of 66

Power Button

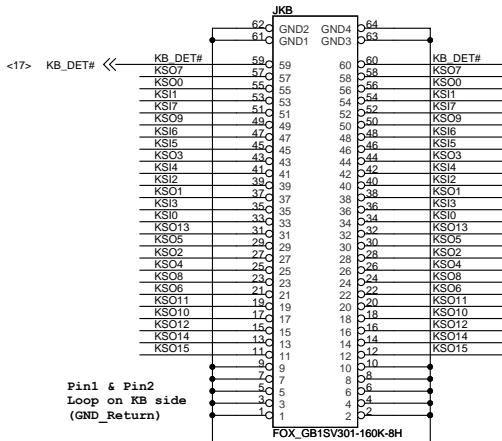
from IO/B PWR BTN

ON/OFF switch (TOP)

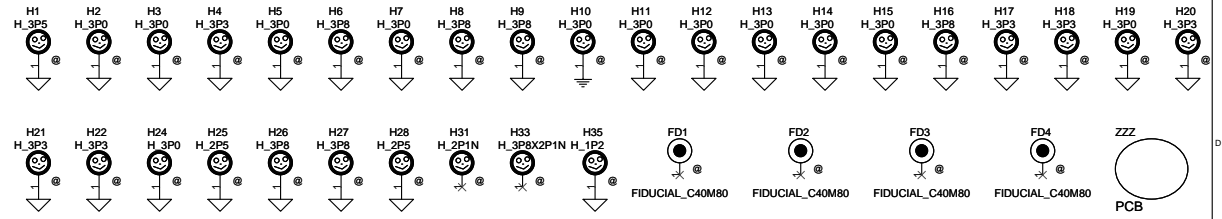
ON/OFF switch (BOT)



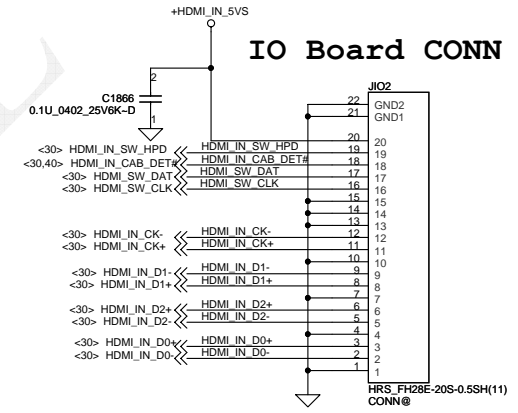
<38,39,40> KS[0..7] <> KS[0..7]
<38,40> KSO[0..15] <> KSO[0..15]



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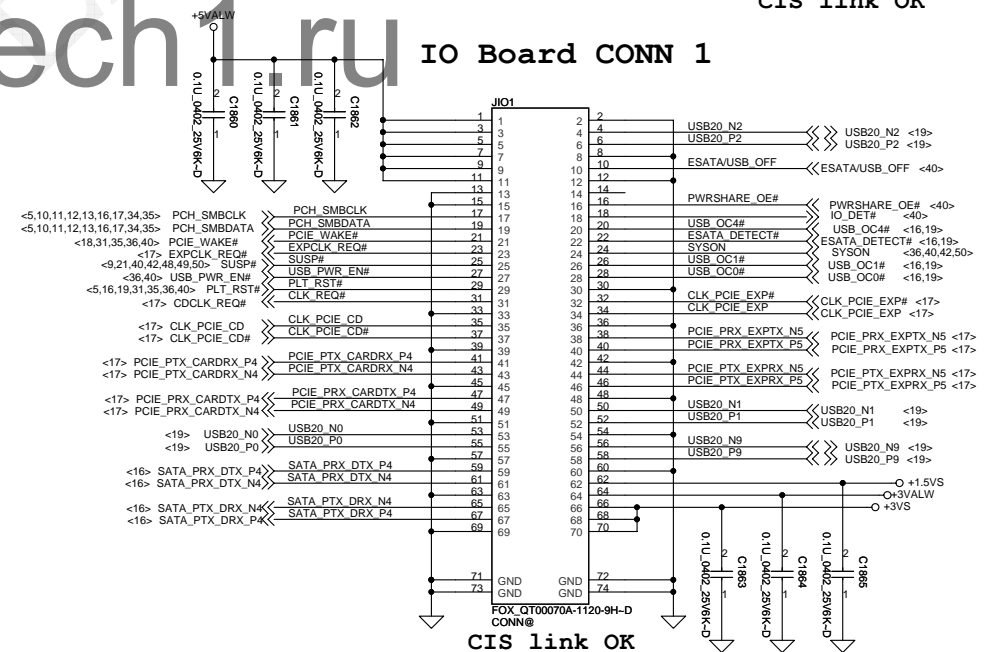


IO Board CONN 2



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IO Board CONN 1



CIS link OK

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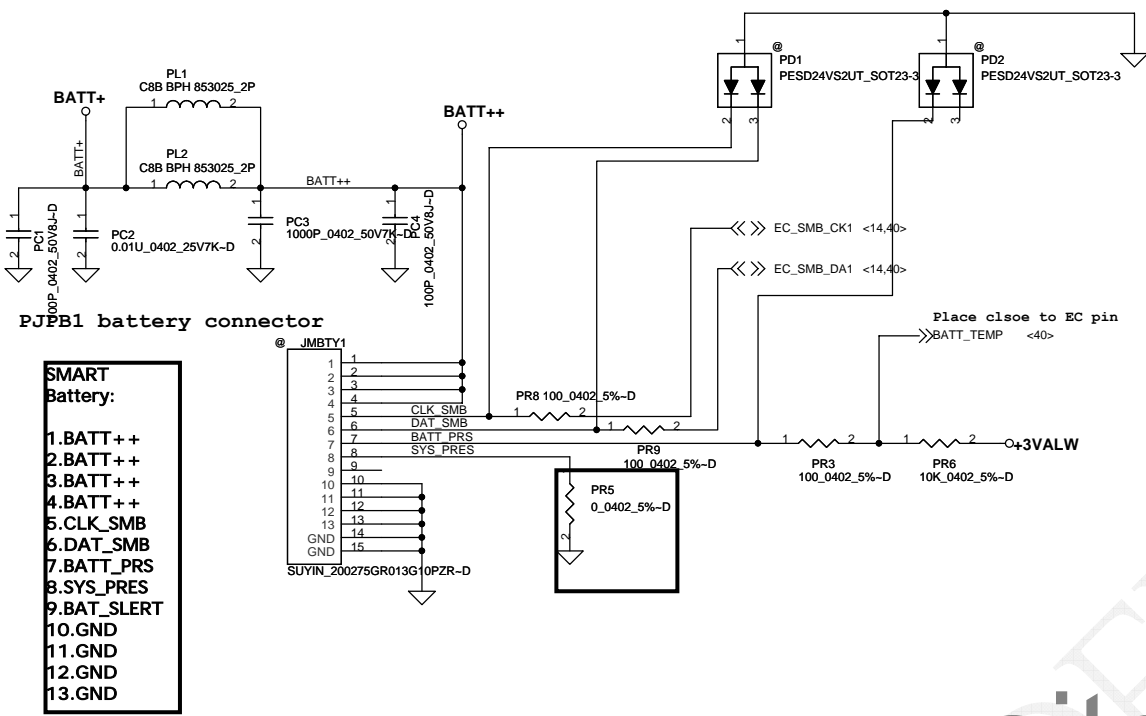
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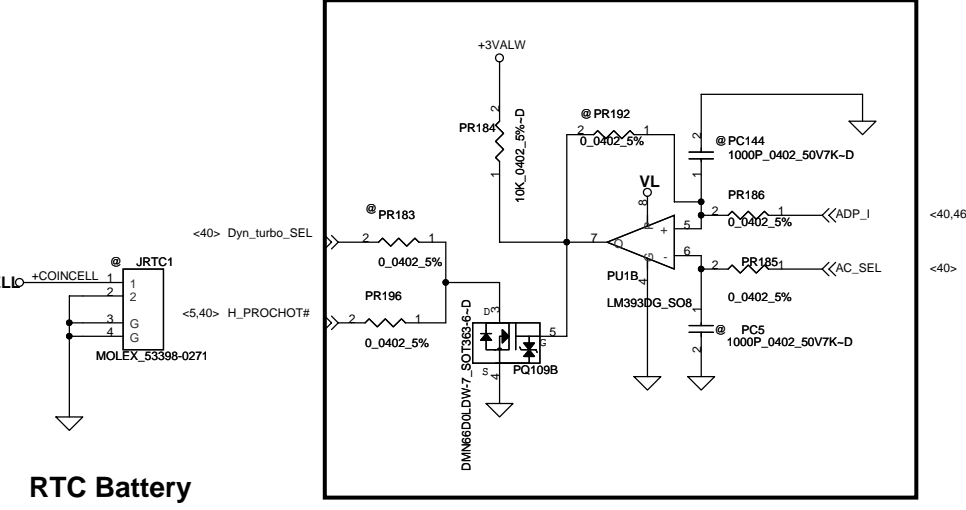
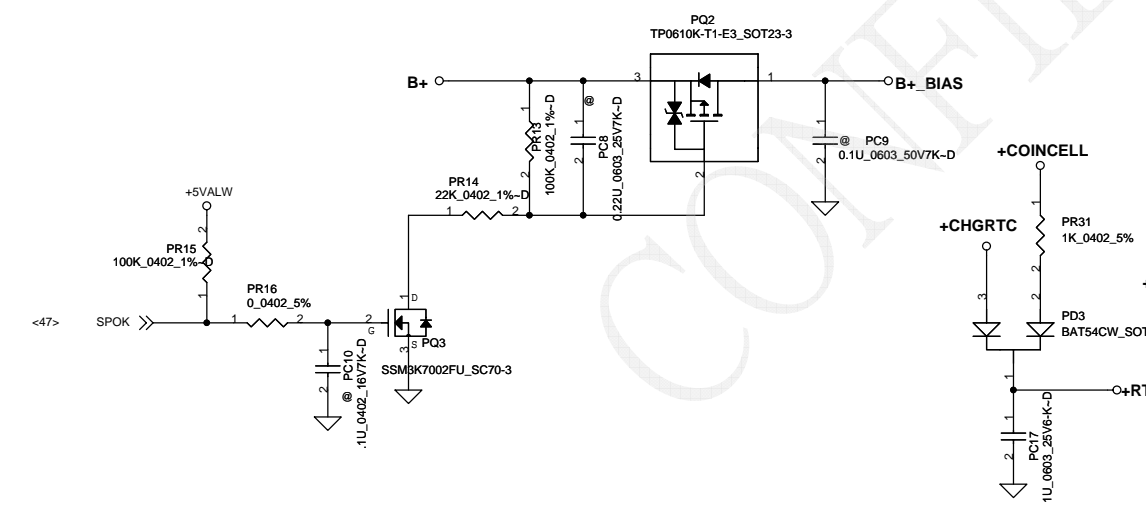
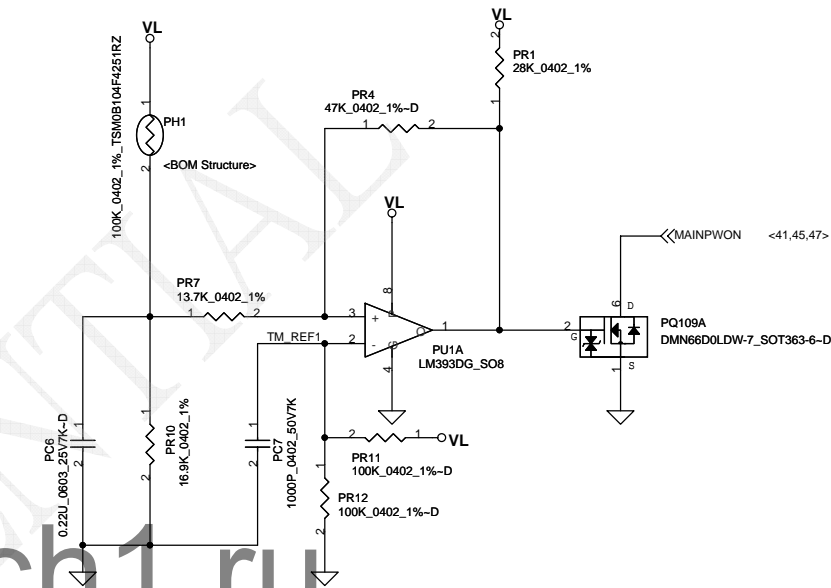
Date: Thursday, December 08, 2011 Sheet 43 of 66

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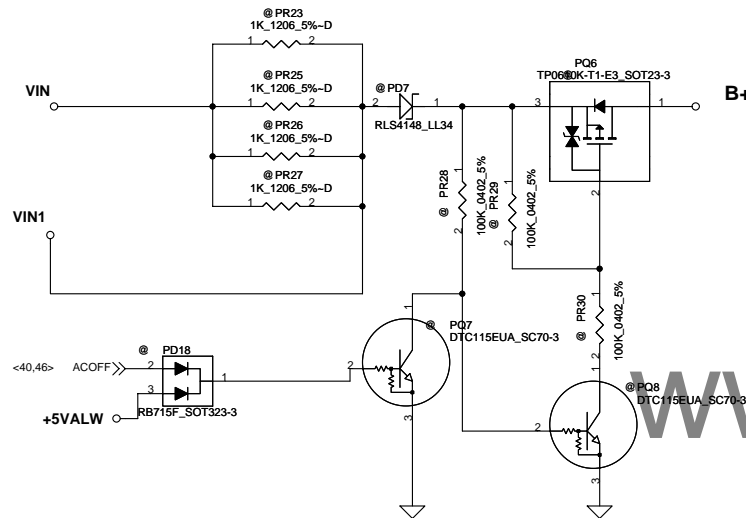
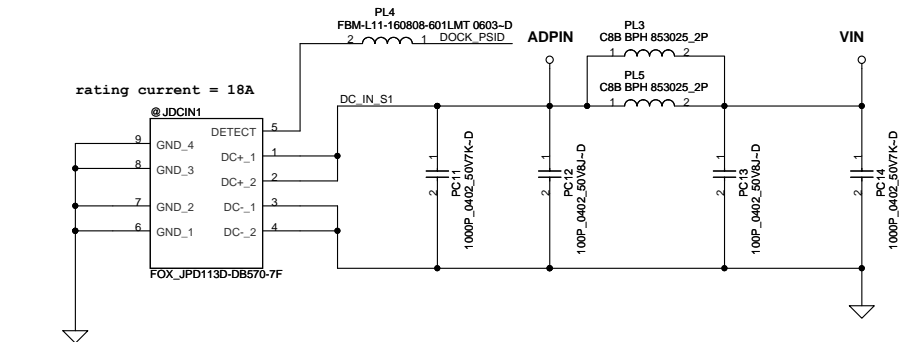


CPU OTP

PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C

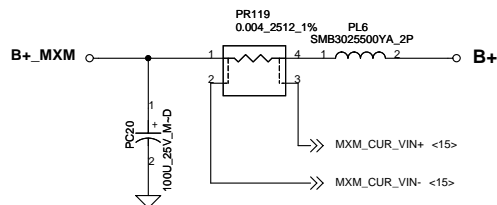
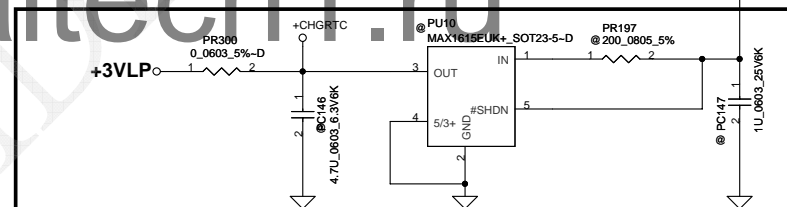
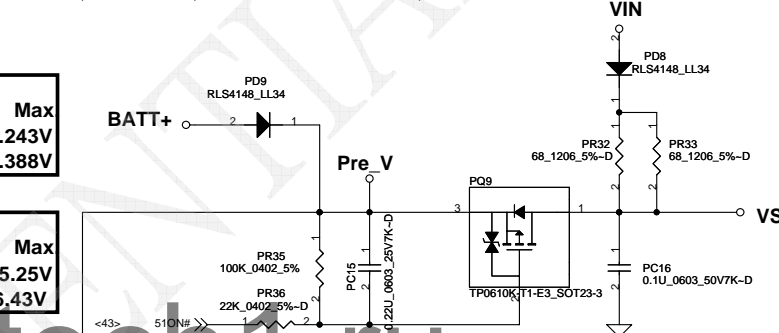
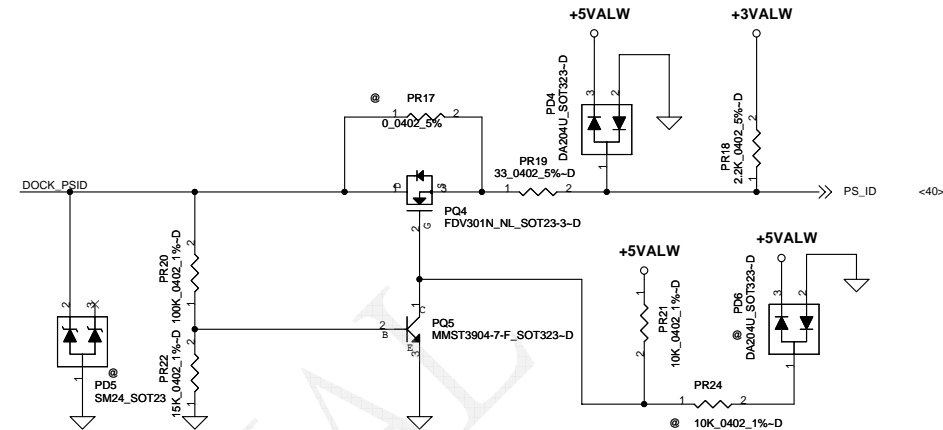


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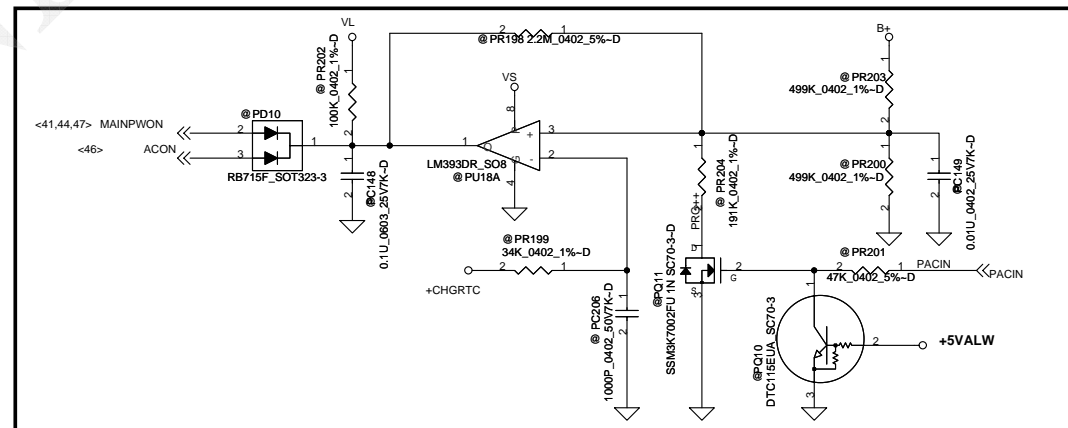
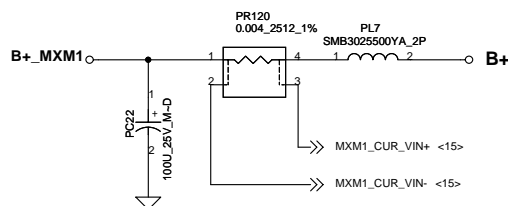


ACIN			
	Min.	typ.	Max
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

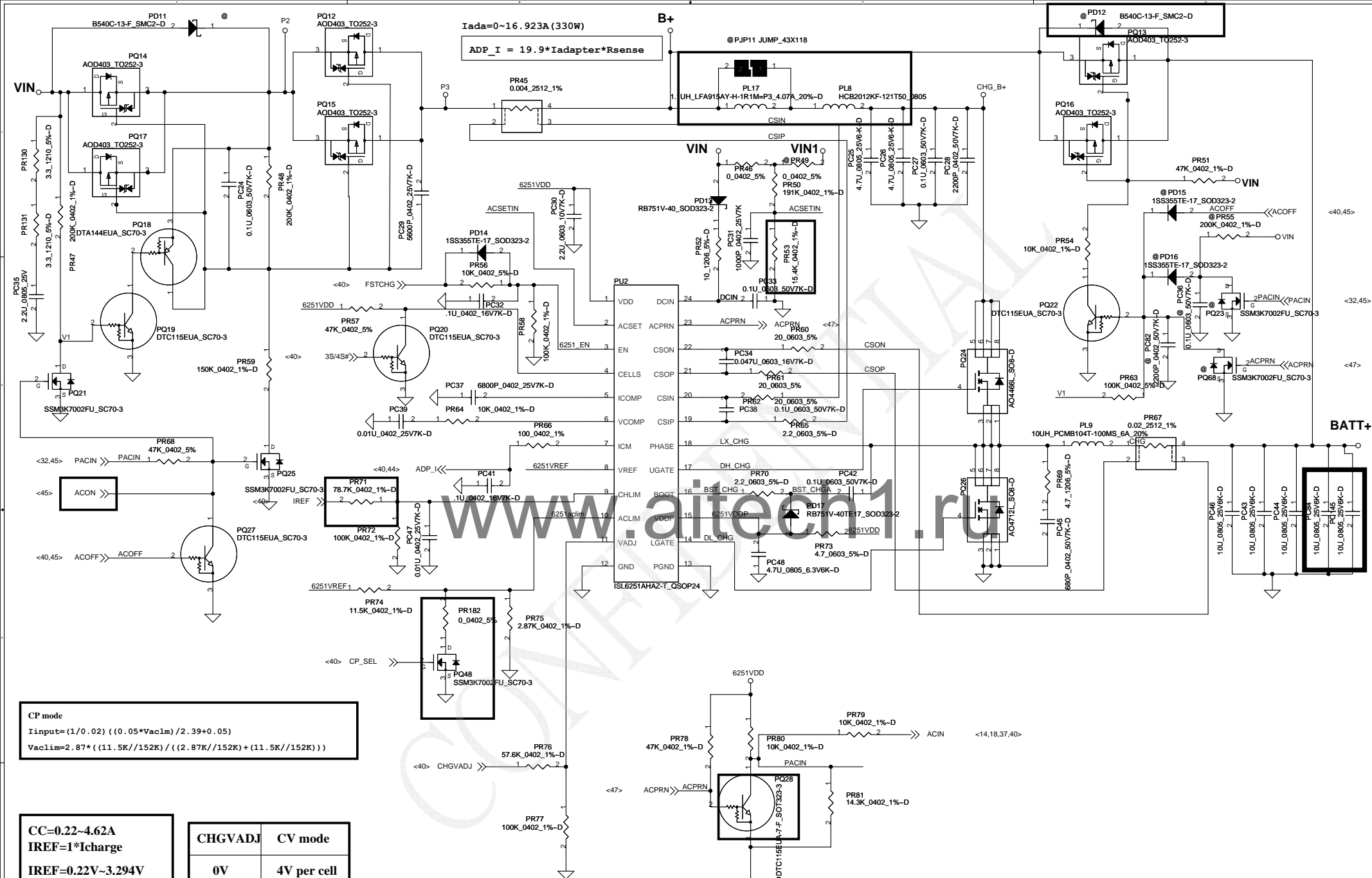
BATT ONLY			
	Min.	typ.	Max
H->L	4.92V	6.1V	5.25V
L->H	6.062V	6.244V	6.43V



For HW request, this is MXM power net



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				Rev	Document Number	Custom
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						Rev C



CP mode
 $I_{input} = (1/0.02) \cdot ((0.05 \cdot V_{acim}) / (2.39 + 0.05))$
 $V_{acim} = 2.87 \cdot ((11.5K / 152K) / ((2.87K / 152K) + (11.5K / 152K)))$

CC=0.22~4.62A
 IREF=1*Icharge
 IREF=0.22V~3.294V

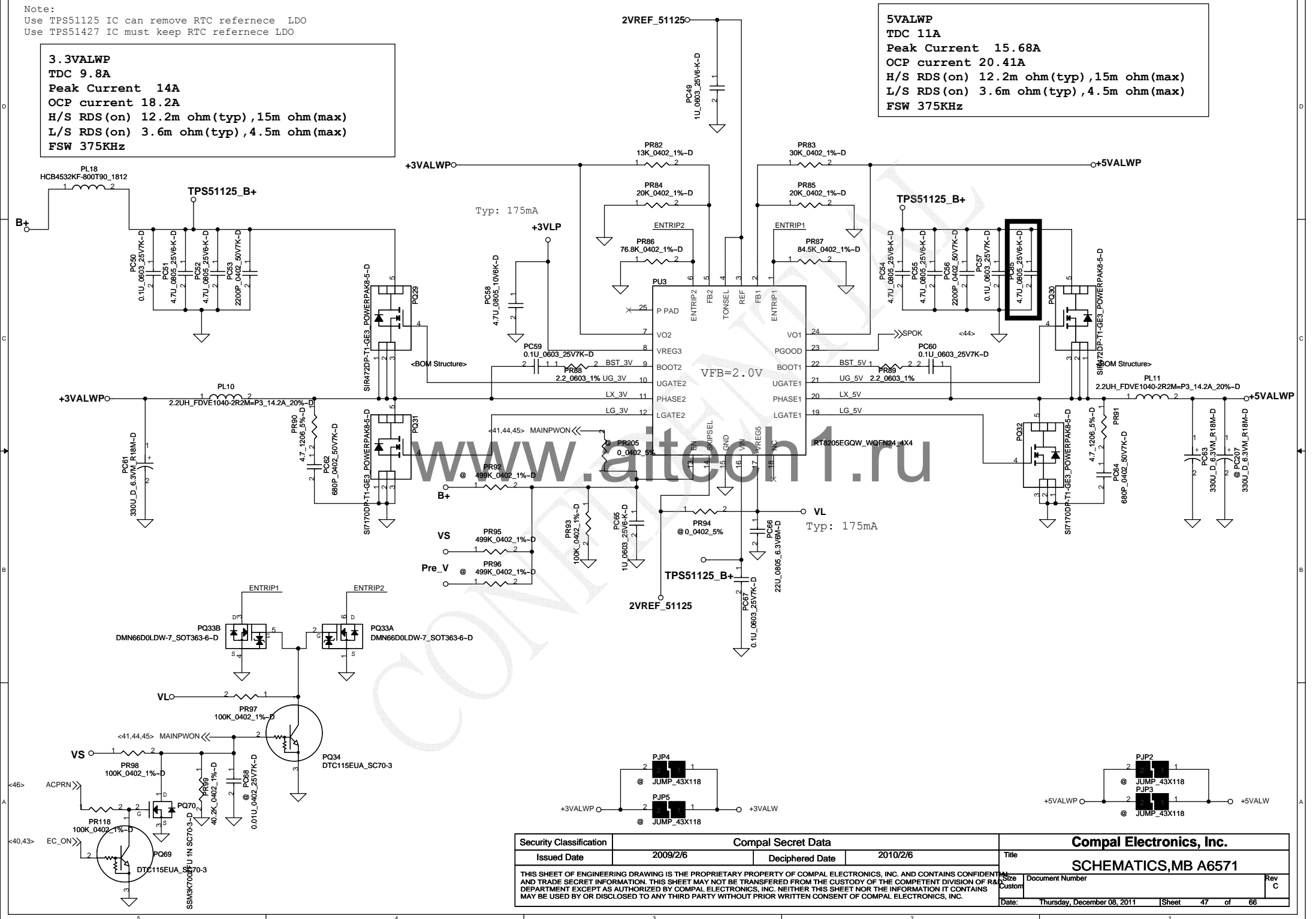
CHGVADJ	CV mode
0V	4V per cell
1.882V	4.2V per cell
3.294V	4.35V per cell

3S/4S# signal	
High	3S
Low	4S

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO

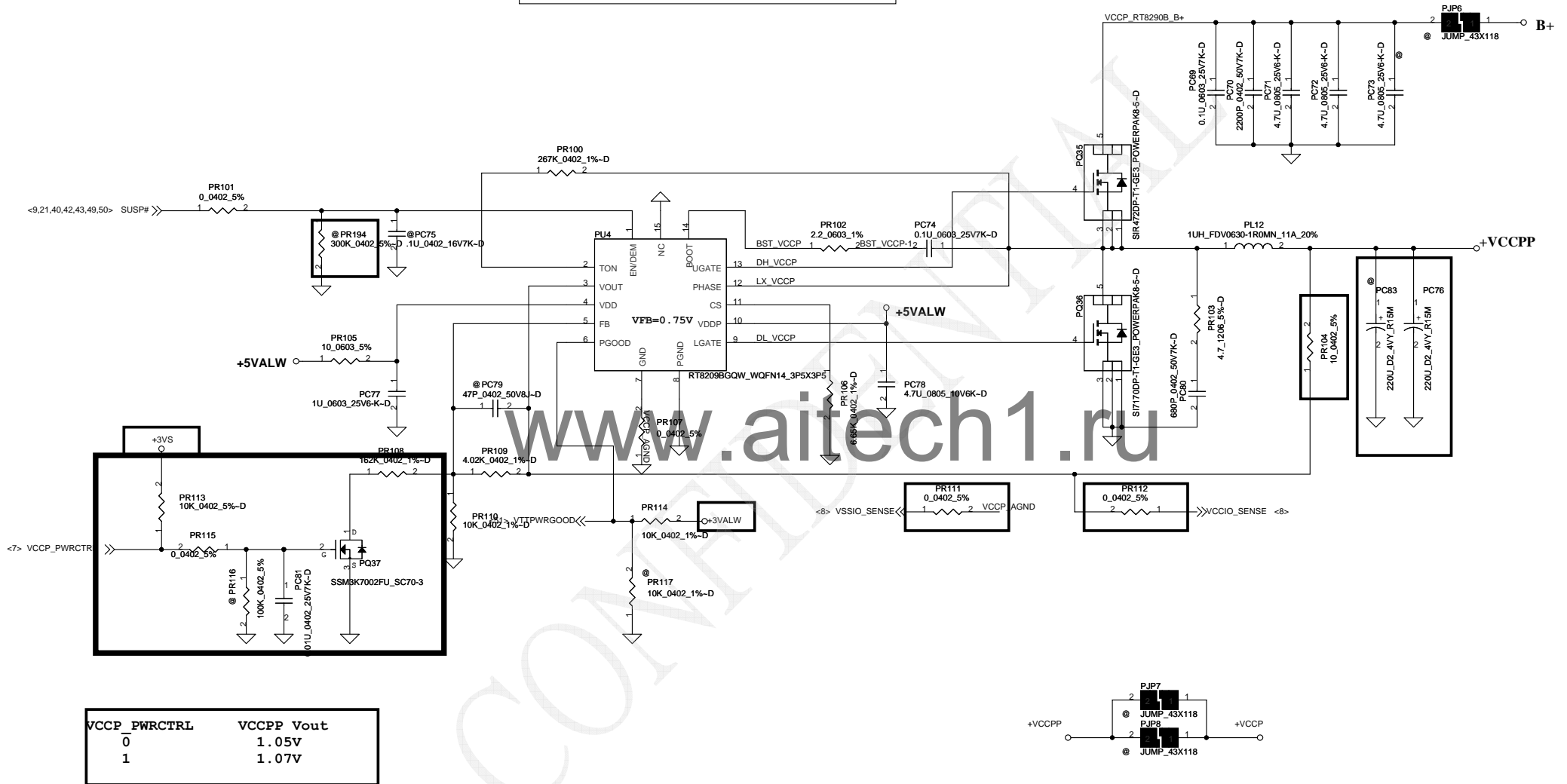
3.3VALWP
 TDC 9.8A
 Peak Current 14A
 OCP current 18.2A
 H/S RDS (on) 12.2m ohm (typ) ,15m ohm (max)
 L/S RDS (on) 3.6m ohm (typ) ,4.5m ohm (max)
 FSW 375KHz

5VALWP
 TDC 11A
 Peak Current 15.68A
 OCP current 20.41A
 H/S RDS (on) 12.2m ohm (typ) ,15m ohm (max)
 L/S RDS (on) 3.6m ohm (typ) ,4.5m ohm (max)
 FSW 375KHz



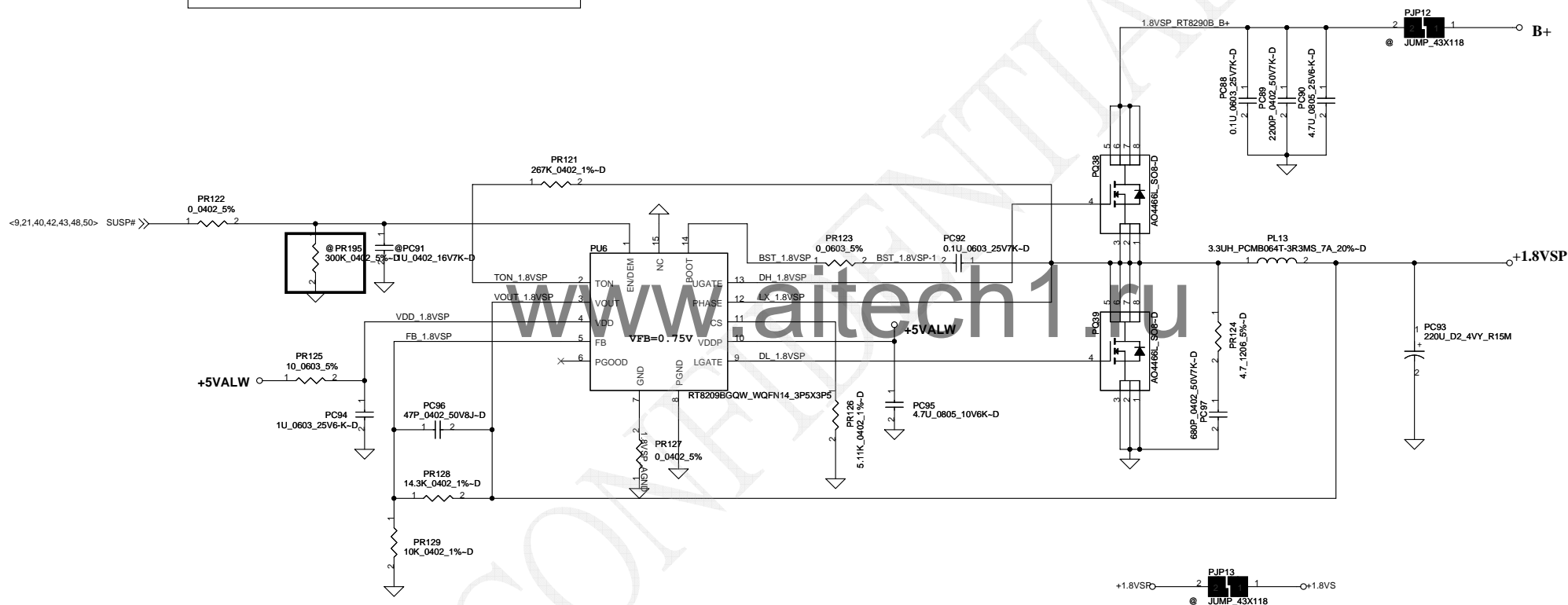
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Issued Date	2009/2/6	Deciphered Date	2010/2/6	Title	
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```
+VCCPP
TDC 8.78A
Peak Current 12.54A
OCP current 16.3A
H/S RDS(on) 12.2m ohm(typ), 15m ohm(max)
L/S RDS(on) 3.6m ohm(typ), 4.5m ohm(max)
FSW 300KHz
```



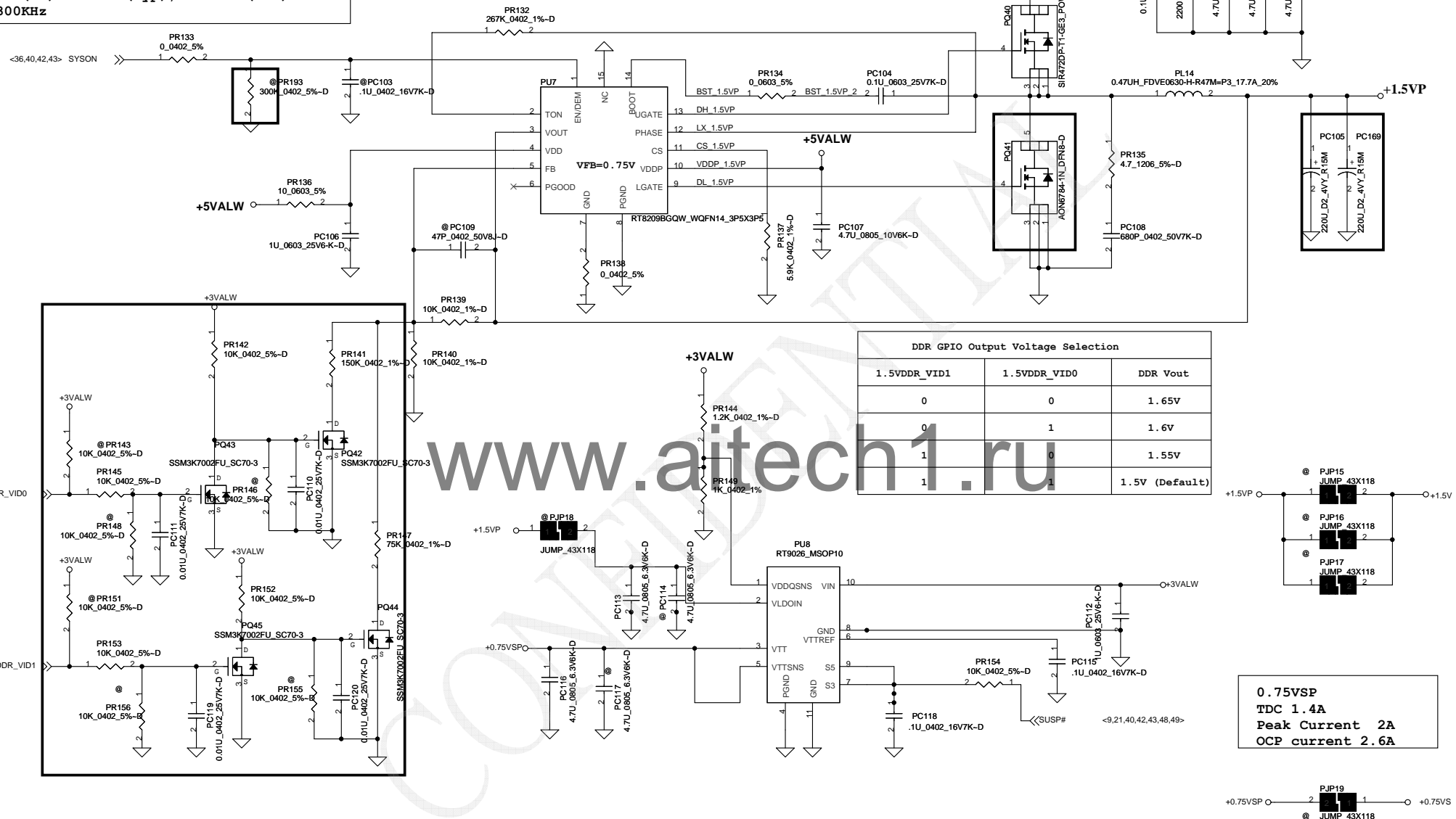
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```
+1.8VSP
TDC 1.015A
Peak Current 1.45A
OCP current 1.9A
H/S RDS(on) 27m ohm(typ), 35m ohm(max)
L/S RDS(on) 27m ohm(typ), 35m ohm(max)
FSW 300KHz
```

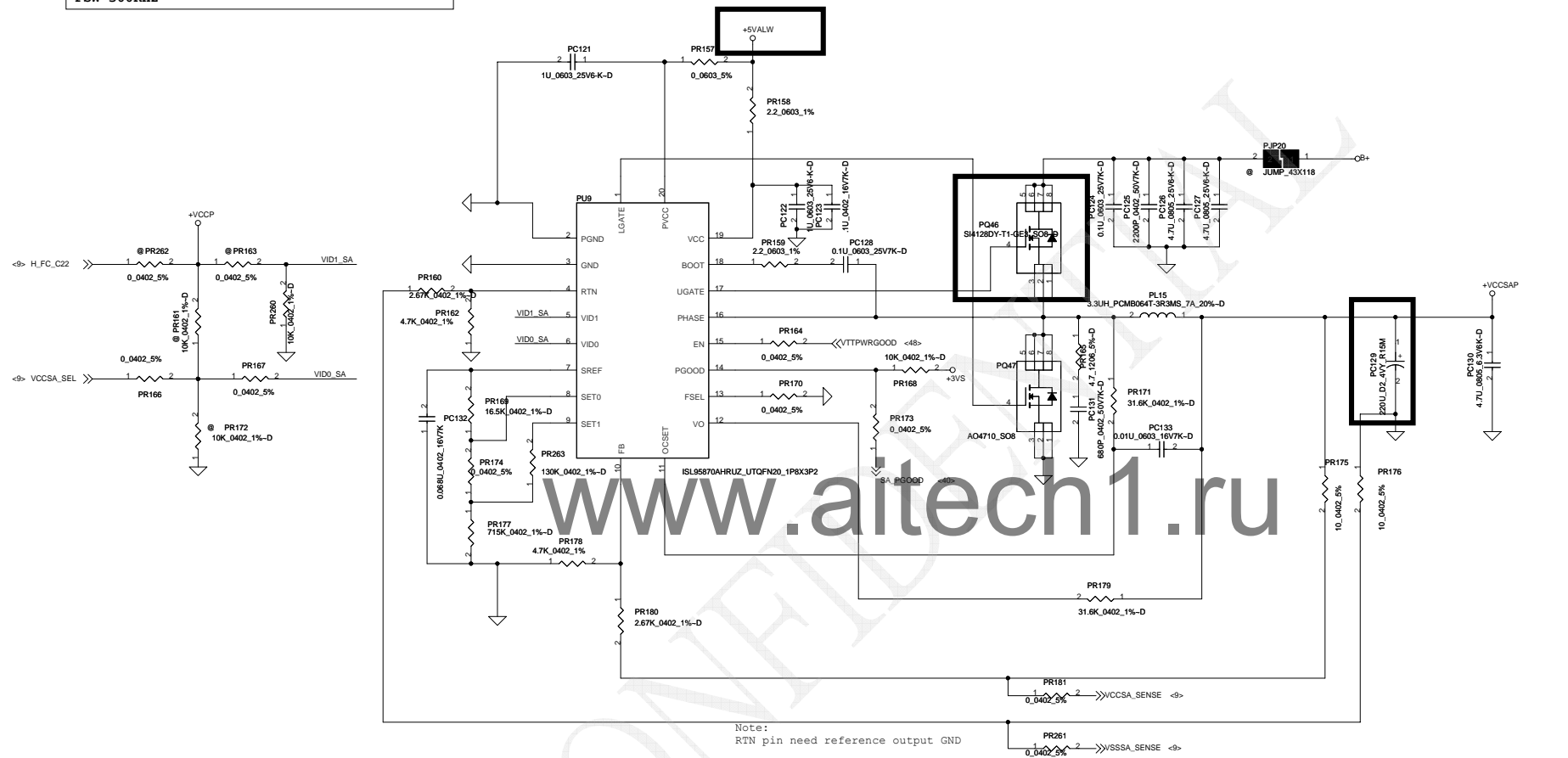


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+1.5VP
TDC 10.42A
Peak Current 14.88A
OCF current 19.34A
H/S RDS(on) 12.2m ohm (typ), 15m ohm (max)
L/S RDS(on) 2.7 ohm (typ), 3.5m ohm (max)
FSW 300KHz



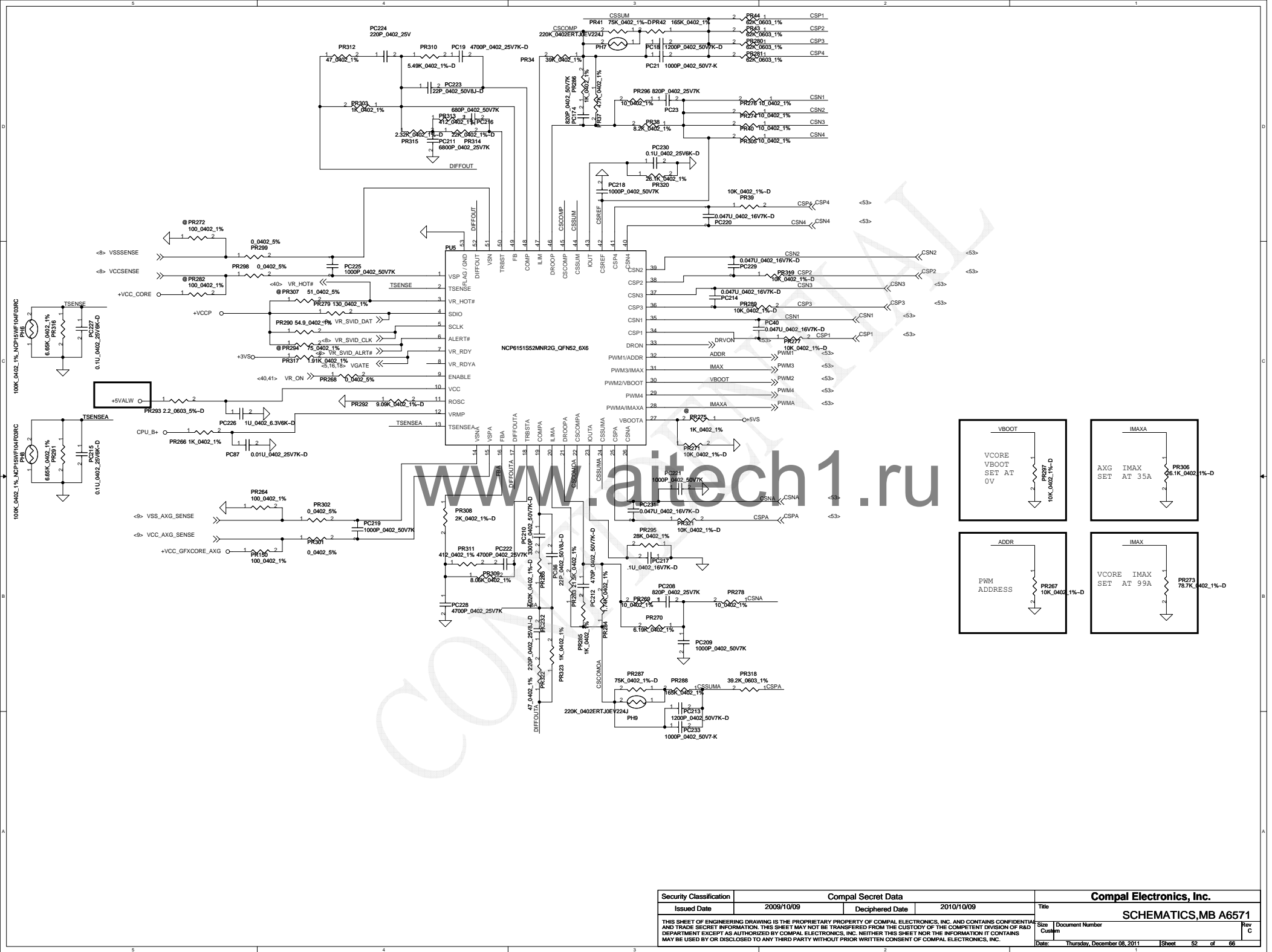
```
+VCCSAP
TDC 4.2A
Peak Current 6A
OCP current 7.8A
H/S RDS(on) 27m ohm(typ), 35m ohm(max)
L/S RDS(on) 11.7 ohm(typ), 14.2m ohm(max)
FSW 300KHz
```

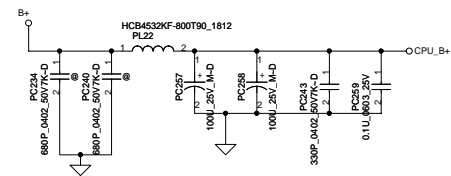
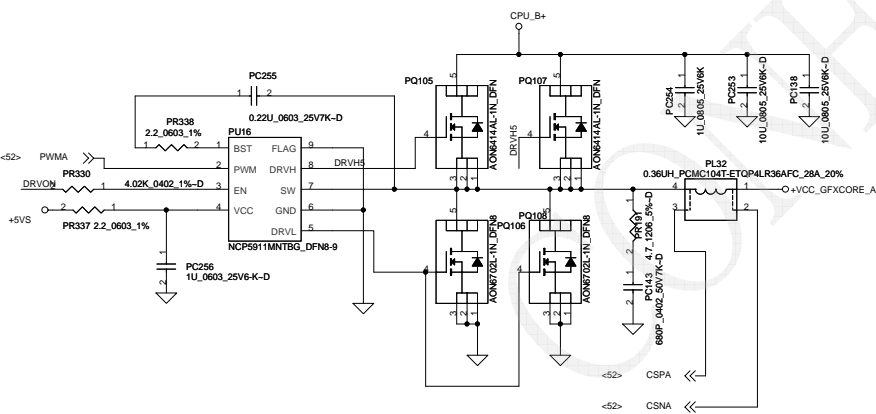
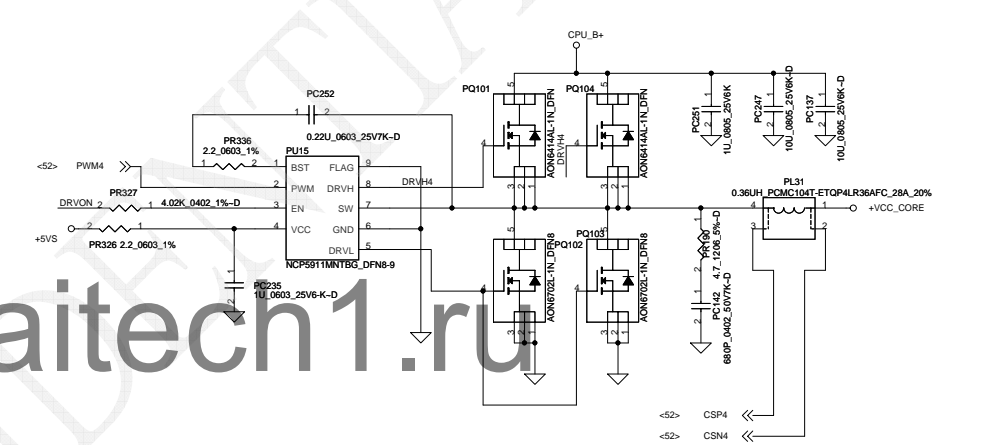
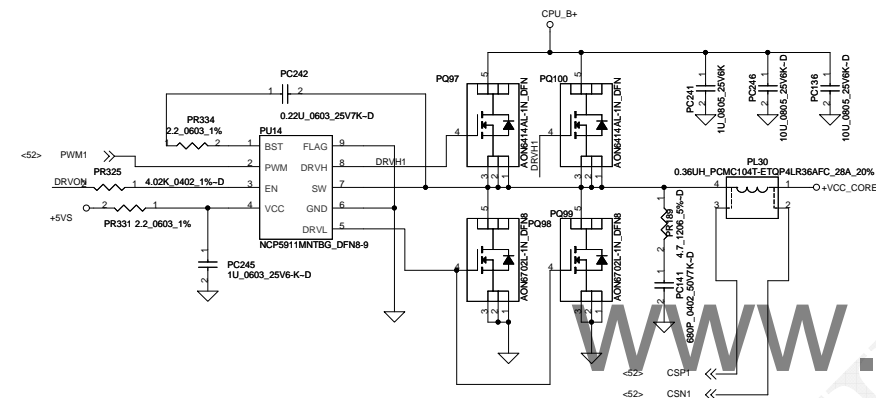
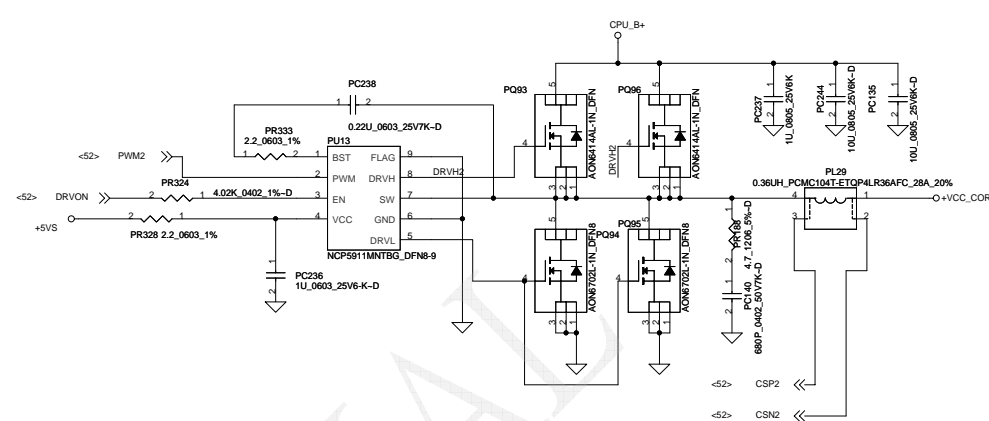
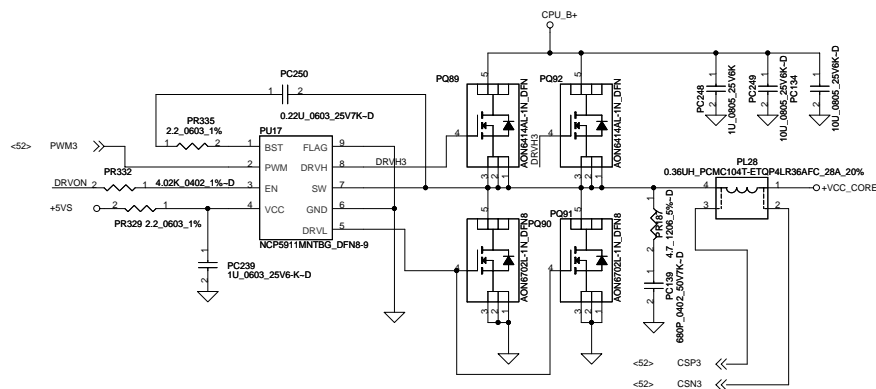


VID0_SA	VID1_SA	VCCSA Vout	Required	
0	0	0.9V	Yes	Yes
1	0	0.8V	Yes	Yes



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1	51	VCCSA_COREP	06/18	Antony	H/S MOS rating enhancement	change PQ46 to SI4128DY	X00
2	46	CHARGER	07/14	Antony	Temperature and voltage rating enhancement	Change PR53 to 15K ohm	X01
3	46	CHARGER	07/14	Antony	output capacitor rating enhancement	Add PC84,PC145 to output	X01
4	47	+5VAWP/+3VALWP	07/14	Antony	input capacitor rating enhancement	Add PC85 to input	X01
5	48	+VCCPP	07/14	Antony	Change resistor size	Change PR104 resistor size to 0402	X01
6	48	+VCCPP	07/14	Antony	Change output capacitor size	Change PC76 to D2 size	X01
7	49	+1.8VSP	07/14	Antony	Change output capacitor size	Change PC93 to D2 size	X01
8	51	VCCSA_COREP	07/14	Antony	Change output capacitor size	Change PC129 to D2 size	X01
9	50	+1.5VSP/0.75VSP	07/14	Antony	Change output capacitor size	Change PC105,PC169 to D2 size	X01
10	44	BATTERY CONN/OTP	10/14	Antony	Follow battery's requirement	Change PR5 from 1K ohm to 0 ohm	X01
11	44	BATTERY CONN/OTP	10/14	Antony	Add power peak function	Add PQ109,PR184,PR185,PR186,PR196 and reserve PR183,PR192,PC144,PC5 space.	X01
12	46	CHARGER	10/14	Antony	Setting charging current to 4.62A	Change PR71 from 150K ohm to 78.7K ohm	X01
13	46	CHARGER	10/14	Antony	Add CP selector circuit	Add PQ48 and PR182	X01
14	46	CHARGER	10/14	Antony	Follow common circuit design	Populate PR55,PC36,PD15,PD16,PQ23 Reserve PR63,PD12,PQ68 space PQ28 use NPN transistor	X01
15	48	+VCCPP	10/14	Antony	Add VID control circuit	Add PR113,PR115,PC81,PQ37,PR108 and reserve PR116 space	X01
16	48	+VCCPP	10/14	Antony	Follow vendor's request	Change PR104 from 0 ohm to 10 ohm, PR111,PR112 from 10 ohm to 0 ohm	X01
17	49	+1.8VSP	10/14	Antony	OCP value meet design setting	Change PR126 from 5.62K ohm to 392 ohm	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
18	49	+1.8VSP	10/14	Antony	Following common circuit	Reserve PR195 space	X01
19	50	+1.5vsp/0.75vsp	10/14	Antony	Following common circuit	Reserve PR193 space	X01
20	50	+1.5vsp/0.75vsp	10/14	Antony	Add VID control circuit	AddPQ42,PQ43,PQ44,PQ45,PR141,PR142,PR145,PR152,PR153,PC110,PC111,PC119,PC120 reserve PR143,PR151,PR156,PR146,PR155 space	X01
21	52	CPU_CORE	10/14	Antony	Change VR solution	Change VR solution from 3+2 to 4+1	X01
22	46	CHARGER	10/14	Antony	Follow EMI request	Add PL8 and reserve PL17 and PJP11 space	X01
23	46	CHARGER	10/14	Antony	For meet temp/volt test SPEC	Change PR53 from 14.3K ohm to 15.4K ohm	X01
24	50	+1.5vsp/0.75vsp	10/18	Antony	sourcer suggest	Change PQ41 to AON6784	X01
25	45	DCIN&DETECTOR	12/08	Antony	Pre-charge disable	un-pop PR23,PR25,PR26,PR27,PR28,PR29, PQ6,PQ7,PQ8,PD18	X02
26	46	CHARGER	12/08	Antony	Pre-charge disable	un-pop PR49,PD15,PD16,PQ23,PQ68,PR55,PC36,PC82 pop PR63	X02
27	45	DCIN&DETECTOR	12/08	Antony	Reservation for the function that Battery can power on without RTC battery.	Reserve PU10,PR197,PC146,PC147 space and pop PR300	X02
28	44	BATTERY CONN/OTP	12/08	Antony	Reservation for the function that Battery can power on without RTC battery.	PD3 pin3 connect to +CHGRTC	X02
29	45	DCIN&DETECTOR	12/08	Antony	Reservation for 15V ac adapter apply	Reserve PU13,PR198,PR199,PR200,PR201,PR202,PR203,PR204,PC148,PC149,PC206,PQ10,PQ11,PD10 space	X02
30	53	VCORE_2	12/08	Antony	Compal common part	Change input capacitor PC237,PC241,PC248,PC251,PC254 to 25V rating voltage.	X02
31	52	VCORE_1	12/08	Antony	Follow intel SVID routing	Change PR279 from 110 ohm to 130 ohm	X02
32	52	VCORE_1	12/08	Antony	Follow intel SVID routing	de-pop PR294	X02
33	52	VCORE_1	12/08	Antony	For CPU loadline setting	Change PR43,PR44,PR280,PR281 from 32.4K ohm to 64.9K ohm	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
34	52	VCORE_1	12/08	Antony	For CPU OCP setting	Change PR34 from 22.6Kohm to 39Kohm, change PR320 from 24.3K to 27K ohm	X02
35	52	VCORE_1	12/08	Antony	For CPU transient setting	Change PR310 from 40.2K ohm to 5.49K ohm	X02
36	52	VCORE_1	12/08	Antony	For GFX loadline setting	Change PR318 from 28Kohm to 39.2Kohm, change PR270 from 3.3K ohm to 6.19K ohm, change PR284 from 6.19K ohm to 1.74K ohm	X02
37	52	VCORE_1	12/08	Antony	For GFX OCP setting	Change PR283 from 15.8Kohm to 21.5Kohm, change PR295 from 24.9K to 28K ohm	X02
38	52	VCORE_1	12/08	Antony	For GFX transient setting	Change PC210 from 2200pF to 3300pF, change PC232 from 100pF to 220pF	X02
39	47	3VALWP/5VALWP	12/21	Antony	Follow EMI request	Reserve PL18 space	X02
40	46	CHARGER	12/22	Antony	Follow EMI request	Add PL17	X02
41	53	VCORE_2	2/16	Antony	Driving capability enhancement	Change PR324,PR325,PR327,PR330,PR332 to 4.02K ohm	A00
42	44	BATTERY CONN/OTP	2/16	Antony	For OTP recovery point setting	Change PR1 to 28K ohm	A00
43	49	1.8VSP	2/16	Antony	Fan out capability enhancement	Change PR126 to 5.11K ohm	A00
44	47	3VALWP/5VALWP	2/16	Antony	Follow common part	Change PQ70 to SSM3K7002FU	A00
45	52	VCORE_1	2/17	Antony	For CPU loadline setting	Change PR43,PR44,PR280,PR281 to 62K ohm	A00
46	52	VCORE_1	2/17	Antony	For CPU transient setting	change PC19 from 3300pF to 4700pF, change PC224 from 100pF to 220pF, change PC223 from 47pF to 22pF, change PC216 from 4700pF to 680pF, change PC211 from 4700pF to 6800pF, change PR315 from 2K ohm to 2.32K ohm	A00
47	47	3VALWP/5VALWP	3/2	Antony	Follow EMI request	Add PL18 (HCB4532KF-900T90_1812) to 3ALWP/5VALWP input side	A00
48	47	3VALWP/5VALWP	3/2	Antony	Follow EMI request	Change PR88,PR89 to 2.2 ohm	A00
49	48	+VCCPP	3/2	Antony	Follow EMI request	Change PR102 to 2.2 ohm	A00
50	51	VCCSAP	3/2	Antony	Follow EMI request	Change PR159to 2.2 ohm	A00
51	52	VCORE_1	3/3	Antony	For 99A +VCC_CORE max current setting	Change PR273 to 78.7K ohm and PR320 to 26.1K ohm	A00
52	52	VCORE_1	3/3	Antony	For 100 degree C VR_HOT threshold setting	Change PR291 and PR316 to 6.65K ohm	A00
53	47	3VALWP/5VALWP	3/8	Antony	Follow EMI request	Delete PJP1	A00

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	5	PROCESSOR(2/6)	2010/8/19	Compal	depop unused part.	Depop RC5, RC6, RC8, CC65, CC66	X01
2	5	PROCESSOR(2/6)	2010/8/19	Compal	follow E3 design, add discharge circuit.	Pop RC64, QC1	X01
3	5	PROCESSOR(2/6)	2010/8/19	Compal	material shortage with SA00003Y000, so we use SA000046R00 on SSI phase.	from SA00003Y000 (S IC 74AHC1G09GW TSSOP 5P OD AND GATE) to SA000046R00 (S IC MC74VHC1G09DFT2G SC70 5P AND)	X01
4	8	PROCESSOR(5/6)	2010/8/19	Compal	derating fail , so change the part to raise voltage tolerance.	change CC107, CC108, CC109 from SGA00001Q80 (S POLY C 330U 2V M D2 LESR6M SX H1.9) to SGA00005H0L (S POLY C 330U 2.5V M D2 LESR6M SX H1.9)	X01
5	9	PROCESSOR(6/6)	2010/8/19	Compal	depop unused part.	Depop UC3, CC179, CC180, RC104, RC107, UC4	X01
6	9	PROCESSOR(6/6)	2010/8/19	Compal	derating fail , so change the part to raise voltage tolerance.	change CC167, CC172, CC176 from SGA00001Q80 (S POLY C 330U 2V M D2 LESR6M SX H1.9) to SGA00005H0L (S POLY C 330U 2.5V M D2 LESR6M SX H1.9)	X01
7	10	DDRIII DIMMA0	2010/8/19	Compal	current SMBUS address can't meet Intel MRD. need to update SMBUS address strap.	Add R1831, R1832, depop RD2	X01
8	10	DDRIII DIMMA0	2010/8/19	Compal	depop unused part.	Depop CD45, CD46, RD15, RD16, RD17, RD18, UD1, UD2	X01
9	11	DDRIII DIMMA0	2010/8/19	Compal	current SMBUS address can't meet Intel MRD. need to update SMBUS address strap.	Add R1833, R1834, depop RD6	X01
10	11	DDRIII DIMMB0	2010/8/19	Compal	depop unused part.	Depop CD49, CD50, RD21, RD22, RD24, RD25, UD3, UD4	X01
11	12	DDRIII DIMMA1	2010/8/19	Compal	current SMBUS address can't meet Intel MRD. need to update SMBUS address strap.	Add R1835 and depop it, pop RD53, depop RD32	X01
12	13	DDRIII DIMMB1	2010/8/19	Compal	current SMBUS address can't meet Intel MRD. need to update SMBUS address strap.	Add R1836 and depop it, pop RD46, depop RD54	X01
13	14	MXM (Master)	2010/8/19	Compal	To fix PACIN will glitch due to backdrive under battery mode issue.	Delete D1, R89, add C1823, U618	X01
14	14	MXM (Master)	2010/8/19	Compal	MXM DP port change, due to NVIDIA MXM card limitation it can't display port A and port B on the same time.	MXM DP Port C change, from DMC to HDMI MXM DP Port A change , from HDMI to DMC	X01
15	14	MXM (Master)	2010/8/19	Compal	derating fail , so change the 0 ohm to Jumper.	Delete R99, add PJP9	X01
16	15	MXM (Slave)	2010/8/19	Compal	derating fail , so change the 0 ohm to Jumper.	Delete R1632, add PJP10	X01
17	15	MXM (Slave)	2010/8/19	Compal	Current sensor circuit review feedback from TI	Depop C1802, C1803, C1804, C1805 Delete R1764, R1767 change R1716, R1720 from 0 ohm to 3.3K	X01
18	15	MXM (Slave)	2010/8/19	Compal	add level shifter for MXM2 SMBUS.	Add Q277, Q278, R1886, R1887	X01

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19	16	PCH (1/8)	2010/8/19	Compal	add net for PCH XDP debug usage.	connect MXM2_PCH_PWR_ON to RH12.1 connect MXM2_PRSENT_R# to RH18.1 connect 1.5VDDR_VID1 to RH5.1 connect ESATA_DETECT# to RH9.1	X01
20	16	PCH (1/8)	2010/8/19	Compal	depop unused part.	Depop RH1, RH3, RH4, RH5, RH6, RH7, RH8, RH9, RH10, RH12, RH13, RH14, RH15, RH16, RH17, RH18, RH19, RH20, RH21	X01
21	16	PCH (1/8)	2010/8/19	Compal	Change resistor value to solve SPI EA fail problem. (voltage min value)	Change RH240 from 0 to 15 ohm	X01
22	16	PCH (1/8)	2010/8/19	Compal	BIOS ROM will be EOL, have to survey new part.	Change U1 from SA00001OZ0L (S IC FL 32MBIT W25X32VSSIG SOIC 8P 3.3V) to SA000046000 (S IC FL 32M W25Q32BVSSIG SOIC 8P SPI ROM)	X01
23	16	PCH (1/8)	2010/8/19	Compal	change Vgs value to ensure the MOS can turn on.	Change QH7 gate pull high power from +3VS to +5VS	X01
24	16	PCH (1/8)	2010/8/19	Compal	follow check list Rev 1.0	from PCH_GPIO22 to ODD_DETECT# (PCH_GPIO36) from ESATA_DETECT# to PCH_GPIO16	X01
25	17	PCH (2/8)	2010/8/19	Compal	To solve backdrive issue on +3VS	Change QH6 pin2 & pin5 pull high power from +3V_PCH to +3VS	X01
27	17	PCH (2/8)	2010/8/19	Compal	Change LID SW control way.	Pop RH162, depop RH172, change R1730.1 from +3V_PCH to +3VALW	X01
28	17	PCH (2/8)	2010/8/19	Compal	Change capacitor value base on KDS EA report	change CH18, CH19 from SE071180J80 (S CER CAP 18P 50V J NPO 0402) to SE071270J8L (S CER CAP 27P 50V J NPO 0402)	X01
29	18	PCH (3/8)	2010/8/19	Compal	original design will cause battery low mode be triggered then system can't boot issue.	Change UH4C.E10 from BT_ACTIVE to PCH_GPIO72 Change RH139.1 & UH4.E10 from PCH_GPIO72 to BATLOW#	X01
30	19	PCH (4/8)	2010/8/19	Compal	change WL_OFF# control pin per EC requirement	Change UH4E.F46 & RPH3.1 from GPIO55 to WL_OFF#	X01
31	19	PCH (4/8)	2010/8/19	Compal	follow Intel check list Rev 1.2	Change RH149 from 1K to 2.2k Change RH150 from 4.7K to 1k	X01
32	19	PCH (6/8)	2010/8/19	Compal	follow Intel CRB	Change RH189 to LH9	X01
33	22	PCH (7/8)	2010/8/19	Compal	follow E3	Change RH208, RH213 from 100 to 10 ohm	X01
34	24	LVDS SW	2010/8/19	Compal	original part (STG3856) body size is too small, it is easy to shift when SMT	Change U3 from SA000039B00 (S IC STG3856QTR QFN 12P SWITCH) to SA000048800 (S IC SN74CB3Q3253PWR TSSOP16P BUS SWITCH)	X01
35	24	LVDS SW	2010/8/19	Compal	material shortage with SA000046P00, so we use SA000048800 on SSI phase.	Change U7, U610 from SA000046P00 (S IC PI3USB14LE TSSOP 16P MUX SWITCH) to SA000048800 (S IC SN74CB3Q3253PWR TSSOP16P BUS SWITCH)	X01
36	24	LVDS SW	2010/8/19	Compal	Correct SSI schematic error design. EMI requirement.	depop RV110,RV112 add R1888, R1889, R1890,C1840, L100	X01

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37	25	LVDS SW	2010/8/19	Compal	this is CMOS pin, needn't pull high.	Depop RV62	X01
38	26	CRT SW	2010/8/19	Compal	Chage filter to solve CRT EA fail issue. (raising time & falling time) Chage filter to solve CRT EA fail issue. (raising time & falling time)	Change CV16, CV17, CV18, CV20, CV21, CV49 from SE00000DB80 (S CER CAP 8P 50V D NPO 0402) to SE00000QB0L (S CER CAP 6.8P 50V D NPO 0402 HIGH-Q) Change , LV1, LV2, LV3 from SM010030380 (S SUPPRE_KC FBMA-L10-160808-600LMT 0603) to SM01000DT0L (S SUPPRE_MURATA BLM18BA220SN1D 0603) from SM010030380 (S SUPPRE_KC FBMA-L10-160808-600LMT 0603) to SM01000DT0L (S SUPPRE_MURATA BLM18BA220SN1D 0603)	X01
39	27	HDMI SW	2010/8/19	Compal	Change HDMI SW and surrounding circuit. add buffer function due to EA fail on SSI	Delete R1746, R1747, R1748, R1749, R1750, R1751, R1752, R1753, R1745, R1744, Q265, Delete R908, R909, R910, R911, R912, R913, R914, R915, R916, R919, R920, Q79 Delete C1186, C1187, C1806, C1807, R1754, R1755, , R1756, R1757, U4 Add R1845,R1846,R1847,R1848,R1849,R1850,R1851,R1852,1853, R1854,R1855,R1856, R1857,R1858,R1859, C1824 Change RV64 from 1M to 1.5M Change RV63 from 470K to 300K Change R461, R462 from 4.7K to 2.2K Change U57 from SA00001DS20 (S IC PI3HDMI412FT-BZHE TQFN 42P DVI/HDMI) to SA00003NB00 (S IC PS8271QFN48GTR-A1 QFN 48P DVI/HDMI)	X01
40	28	DP SW	2010/8/19	Compal	There is only one 2.2uF_0402 cap in BOM. To simplify BOM, chagne to 0603.	Chage filter to solve CRT EA fail issue. (raising time & falling time)	X01
41	28	DP SW	2010/8/19	Compal	SSI schematic is for standard type, not mini type DP.	update JDP pin define, follow mini DP type specification	X01
42	29	DMC SW	2010/8/19	Compal	Change HDMI SW and surrounding circuit. add buffer function due to EA fail on SSI	Delete R1763, R1764, R1765, R1766, R1767, R1768, R1769, R1770, R1759, R1760, R1761, Delete R941, R942, R944, R946, R947, R950, R951, R952, R948, R949, Q97 R1762, Delete C1188, C1189, C1808, C1809, R1236, R1237, U5, R1762, R1779, R1780, R1781, U5 Add R1860, R1861, R1862, R1863, R1864, R1865, 1866, R1867, R1868, R1869, R1870, R1871, R1872, R1873, R1874, C1825 Change U132 from SA00001DS20 (S IC PI3HDMI412FT-BZHE TQFN 42P DVI/HDMI) to SA00003NB00 (S IC PS8271QFN48GTR-A1 QFN 48P DVI/HDMI)	X01
43	30	HDMI IN	2010/8/19	Compal	add I2S path for DAC. add new GPIO pin to codec. add I2C bus for LCD EDID reading. change SMBUS path form PCH to EC follow ST schematic review suggestion. material shortage with SA00001YI00, so we use SA024020710 on SSI phase. base on crystal EA report to fine tune cap value.	Add R1782, R1783, R1876, R1877, R1880, R1881,R1882, R1891 Delete C810, Change U614 from SA00001YI00 (S IC EE 2K AT24C02BN-SH-T SO 8P) , and depop it. to SA00003ND00 (S IC EE 2KX8 M24C16-WMN6TP SO 8P) Change U9 from SA00001YI00 (S IC EE 2K AT24C02BN-SH-T SO 8P) to SA024020710 (S IC EE 256X8 M24C02-WMN6TP SO 8P) Change C1750, C1751 from 10pF to 22pF	X01

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44	31	GLAN	2010/8/19	Compal	base on crystal EA report to fine tune cap value.	Change CL18, CL19 from SE071270J80 (S CER CAP 27P 50V J NPO 0402) to SE071180J8L (S CER CAP 18P 50V J NPO 0402)	X01
45	31	GLAN	2010/8/19	Compal	change RL19 to raise Vgs value.	Change RL19 from 470K to 300K	X01
46	31	GLAN	2010/8/19	Compal	depop unused part.	Depop RL7	X01
47	32	Codec	2010/8/19	Compal	follow safty team's recommend	Change D31, D32, D34 from SCA00000J0L (S ZEN ROW SM05T1G 3P C/A SOT23) to SCA00001100 (S ZEN ROW PJDLC05C 3P C/A SOT23)	X01
48	32	Codec	2010/8/19	Compal	follow EMI requirement.	Add R1838, R1839, C1831, C1832, C1833, C1834, C1835, L99, pop R1792	X01
49	32	Codec	2010/8/19	Compal	we use SA000047R00 on SSI phase, control by memo, now implement it.	Change U10, U13 from SA000045J0L (S IC MAX9724AETC+T TQFN-EP 12P HP AMP) to SA000047R00 (S IC MAX9724BETC+T TQFN-EP 12P HP AMP)	X01
50	32	Codec	2010/8/19	Compal	it's duplicated circuit design on audio mute# schematic, so we can remove one set.	Delete R980 C1087, C1118, R1219, U58, U61, add R1840	X01
51	32	Codec	2010/8/19	Compal	add DAC and the surrounding circuit to solve HDMI IN 44.1KHz sample rate issue.	Add C1826, C1827, C1828, C1829, C1830, R1883, R1884, C1836, C1837, C1838, C1839, R1892, R1893, R1894, R1895, U4	X01
52	32	Codec	2010/8/19	Compal	add GPIO pin that let ST6038 inform codec HDMI IN audio signal will be sent out	connect U11 pin 30 to U2 pin 127	X01
53	33	Sub woofer /Speaker AMP	2010/8/19	Compal	follow safty team's recommend	Change D21, D22, D61, D63 from SCA00000T00 (S ZEN ROW PESD5V0U2BT 3P C/C SOT23 ESD) to SCA00001100 (S ZEN ROW PJDLC05C 3P C/A SOT23)	X01
54	33	Sub woofer /Speaker AMP	2010/8/19	Compal	To solve SPDIF function doesn't work issue.	Change C740, delete R721, R722	X01
55	33	Sub woofer /Speaker AMP	2010/8/19	Compal	update Audio Amp gain setting according to Audio team's requiriment.	Change C1097 from 0.047uF to 0.1uF; R1194 from 11.5K to 4.75K	X01
56	33	Sub woofer /Speaker AMP	2010/8/19	Compal	Follow IDT review suggestion.	Change C738, C739 from SE00000698L (S CER CAP 1U 25V K X5R 0603) to SGA00001E0L (S POLY C 150U 6.3V M B2 LESR45M PSL H1.9) Delete C742, C743, L91, L92	X01
57	34	SATA HDD & FFS	2010/8/19	Compal	change part for derating improved	Change RS7 from 470K to 300K Change CS28 from SE076104K8L (S CER CAP .1U 16V K X7R 0402) to SE00000G88L (S CER CAP 0.1U 25V K X5R 0402)	X01

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58	35	Mini Card WLAN/BT/DMC	2010/8/19	Compal	old circuit will cause battery low mode be triggered then system can't boot issue.	Change JBT.6 from BT_ACTIVE to NC	X01
59	36	USB 3.0	2010/8/19	Compal	USB 3.0 IC version change, reserve 0 ohm for prior SMI pin.	Add R1843 and depop it, add R1844	X01
60	36	USB 3.0	2010/8/19	Compal	base on crystal EA report to fine tune cap value.	Change C801 from 12pF to 15pF	X01
61	36	USB 3.0	2010/8/19	Compal	we use SA000046000 on SSI phase, control by memo, now implement it.	Change U53 from SA00003NH0L (S IC FL 512K AT25F512B-SSH-T SOIC 8P) to SA000046000 (S IC FL 512K MX25L5121EMC-20G SOP 8P)	X01
62	36	USB 3.0	2010/8/19	Compal	USB power switch can't be turn off under S3/S4.	change U42 pin3 , U45 pin 3 from SYSON# to USB_PWR_EN#	X01
63	37	ELC (1)	2010/8/19	Compal	schematic design error on SSI, update it to solve hall sensor can't work issue.	change U42 pin3 , U45 pin 3 from SYSON# to USB_PWR_EN#	X01
64	37	ELC (1)	2010/8/19	Compal	Use different CPN control each boot loader individually	change U602 from SA00003IR00 (S IC C8051F347-GQ LQFP 32P USB FLASH MCU) to SA00003IR30 (S IC C8051F347-GQ LQFP 32P MCU PAR10)	X01
65	37	ELC (1)	2010/8/19	Compal	Add diode for block backdrive.	Add D70, R1841	X01
66	37	ELC (1)	2010/8/19	Compal	Old part will be EOL.	change U604 from SA00000XT00 (S IC FL 8M MX25L8005M2C-15G SOP 8P) to SA00001V400 (S IC FL 8M EN25F80-75HCP SOIC 8P)	X01
67	37	ELC (1)	2010/8/19	Compal	Change part for derating improved	Add R1842 Change Capacitor voltage to tolerance	X01
68	38	ELC (2)	2010/8/19	Compal	follow EMI team requirement.	Change D27 from SCA00000T00 (S ZEN ROW PESD5V0U2BT 3P C/C SOT23 ESD) to SCA00001100 (S ZEN ROW PJDLCO5C 3P C/A SOT23)	X01
69	38	ELC (2)	2010/8/19	Compal	schematic design error on SSI, update it to solve hall sensor can't work issue.	change JTP.7, Q222.2 from LID_SW# to LID_SW_IN#	X01
70	38	ELC (2)	2010/8/20	Compal	Change part for derating improved	Change C1756 from SE076104K8L (S CER CAP .1U 16V K X7R 0402) to SE00000G88L (S CER CAP 0.1U 25V K X5R 0402) Change R1643 from 100K to 1.5M, R1660 from 470K to 300K	X01
71	38	ELC (2)	2010/8/20	Compal	To reduce the footprint size.	Change Q217~Q222 to Q217, Q272, Q273 from SB570020110 (S TR 2N7002E-T1-E3 1N SOT23) to SB57002528L (S TR 2N7002DW-7-F 2N SOT-363)	X01

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72	40	EC KB930	2010/8/19	Compal	follow EC team comment, update GPIO	U14.101 from SCR_LED# to MXM2_FAN_FB U14.106 from NC to SCR_LED# U14.28 from ALERT1# to SYSTEM_FAN_FB U14.29 from PCH_PWR_EN to MXM1_FAN_FB U14.93 from SYS_SHDN# to PCH_PWR_EN U14.108 from NC to EC_LID_OUT# U14.70 from EC_LID_OUT# to AC_SEL U44.16 from NC o CP_SEL U44.19 from NC to EC_AC_BAT# U44.8 from NC to DYN_TURBO_SEL U44.7 from NC to HDMI_IN_CAB_DET U44.5 from USB_DET#_DELAY to USB_PWR_EN#	X01
73	40	EC KB930	2010/8/19	Compal	base on crystal EA report to fine tune cap value.	Change C545, C546 from SE071150J80 (S CER CAP 15P 50V J NPO 0402) to SE071270J8L (S CER CAP 27P 50V J NPO 0402)	X01
74	40	EC KB930	2010/8/19	Compal	Change Crystal to internal CLK.	Pop R511, depop R545, R546, X1, add R1885	X01
75	40	EC KB930	2010/8/19	Compal	Change Board ID to X01	Change R466 from 0 ohm to 8.2K	X01
76	41	Thermal Sensor & FAN control	2010/8/19	Compal	Change FAN controller IC and surrounding circuit.	Change U615, U616, U617 from EMC 2113 to EMC1412 Change R1821 from 10K to 15K Delete R1799, R1809, R1818, R1795, R1804 Add Q274,Q275,Q276	X01
77	42	DC/DC Interface	2010/8/19	Compal	Change part for derating improved	Change U20 from SB00000HZ00 (S TR AO4478L 1N SO8) to SB00000L800 (S TR AO4728L 1N SOIC-8) Change R1484 from 0 ohm to 100K, and pop it. Change R1541 from 10K ohm to 0 ohm	X01
78	43	IO CONN / KB	2010/8/19	Compal	depop unused part.	Depop C558~C583	X01
79	43	IO CONN / KB	2010/8/20	Compal	IO board layout change, so change JIO2 pin define.	JIO2.2 from HDMI_IN_D2+ to HDMI_IN_D0- JIO2.3 from HDMI_IN_D2- to HDMI_IN_D0+ JIO2.5 from HDMI_IN_D1+ to HDMI_IN_D2- JIO2.6 from HDMI_IN_D1- to HDMI_IN_D2+ JIO2.8 from HDMI_IN_D0+ to HDMI_IN_D1+ JIO2.9 from HDMI_IN_D0- to HDMI_IN_D1-	X01

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80	25, 40	IO CONN / KB	2010/11/25	Compal	Implement LCD backlight control circuit, leverage Voyager design.	rename LCD_BKL_EN# to LCD_BKL_EN add Q44, Q45, C340, C346, R422, R423 delete Q281, Q282, C1867, C1868, C1869, R1909 depop LV9	X02
81	5	PROCESSOR(2/6) PM,XDP,CLK	2010/11/29	Compal	current power sequence violate Intel spec, update circuit to fix it.	add RC58 depop R1905	X02
82	26	CRT SW	2010/11/29	Compal	Follow EMI team's requirement, change bead	change LV1, LV2, LV3 From SM01000BP00 (S SUPPRE_ MURATA BLM18BB050SN1D 0603) To SM01000AO0L (S SUPPRE_ MURATA BLM18BB750SN1D 0603)	X02
83	24, 32	LVDS SW - GPU & PCH HD Audio_IDT92HD73C				change L94, L100 From SM01000CY00 (S SUPPRE_ KC FBMA-10-100505-301T 0402) To SM01000BV0L (S SUPPRE_ MURATA BLM15BB221SN1D 0402)	X02
84	43	IO/B CONN / KB	2010/12/6	Compal	remove unused USB changer circuit.	delete U63, Q57, D51, D52, D58, R1143, R1144, R1145, R1238, C1150, C1151 rename JIO1 pin 14 to NC	X02
85	39	ELC (3)	2010/12/6	Compal	ME reverse JKPBL to solve hard assembly issue.	reverse JKPBL pin define.	X02
86	43	IO CONN / KB	2010/12/6	Compal	ME change connector to solve hard assembly issue.	change JKP from MOLEX_52610-1075 to ACES_50611-0100N-001 change JKB from FOX_GB1SV301-160K-8H to AMPHE_G28301021AHR change JIO2 from TYCO_2-1734820-0 to HRS_FH28E-20S-0.5SH(11)	X02
87	27	HDMI SW	2010/12/6	Compal	follow PSL.	change L55, L57, L58, L59 from SM070000K00 (S COM FI_ KINGCORE WCM-2012-900T) to SM070001E0L (S COM FI_ MURATA DLW21SN900HQ2L)	X02
88	16	PCH (1/8) SATA,HDA,SPI, LPC	2010/12/9	Compal	add for EC enable / disable ME function.	pop RH50	X02
89	32	HD Audio_IDT92HD73C	2010/12/17	Compal	HDMI IN Audio detect issue, follow Voyager design.	add R1913, R1914 and reserve R1914	X02
90	34	SATA HDD & ODD & FFS	2010/12/17	Compal	SATA EA - Gen3 Peak to Peak Jitter Fail	rename JHDD even number pins to NC pin. modify SATA connector routing to reduce signal reflection.	X02
91	32	HD Audio_IDT92HD73C	2010/12/17	Compal	change capacitor size to improve THD+N value of Audio Precision EA	change C336, C337, C355, C359 form 0603 to 0805	X02
92	32	SATA HDD & ODD & FFS	2010/12/17	Compal	follow IDT review feedback.	change C345 from 1000pF to 1uF change Q280 pin1 & pin4 from GND to GNDA change JSPDIF pin2 from GNDA to GND	X02
93	40	EC ENE-KB930	2010/12/17	Compal	change Board ID	change R466 from 18K to 33K	X02

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94	32	HD Audio	2011/2/21	Compal	Reduce ripple of Codec DVDD_IO	change R247 to L5 SM010005500 (S SUPPRE_ MURATA BLM18AG601SN1D 0603) [ST implemented through memo]	A00
95	32	HD Audio	2011/2/21	Compal	To solve po noise when resume from S3/S4/S5	pop U620, U621, C1845, C1846. [ST implemented through memo]	A00
96	37	ELC (1)	2011/2/21	Compal	ELC lost during power on/off test.	Pop R1575, depop R1572 [ST implemented through memo]	A00
97	33, 38	Speaker AMP / ELC (2)	2011/2/21	Compal	follow Safty team's suggestion.	Pop D27, change D21, D22 to SCA00000E10 (S ZEN ROW PJSOT24CH 3P C/A SOT-23) [ST implemented through memo]	A00
98	40	EC ENE-KB930	2011/2/11	Compal	change Board ID	change R466 from 33K to 56K	A00
99	16-23	PCH	2011/2/11	Compal	change PCH to B3 stepping	change UH4 from SA00004ED1L to SA00004ED5L	A00
100	43	IO/B CONN / KB	2011/2/11	Compal	take off reserved Swith button	depop SW1, SW2	A00
101	25	LVDS SW	2011/2/15	Compal	add diode on EC pin 105 for EOS protection.	add R1918, change RV43 to D73	A00
102	24, 30	HDMI IN	2011/2/15	Compal	I2C of HDMI IN Scalar caued LCD EDID crash.	add RV64~RV67 depop R1880, R1881	A00
103	24, 25	LVDS SW	2011/2/15	Compal	LCD displayed noise when +3VALW down to 90%	change QV12 to SB00000H50L	A00
104	37	ELC (1)	2011/2/15	Compal	ELC lost during power on/off test.	add C1730, 1uF on U602 reset pin	A00
105	21	PCH	2011/2/15	Compal	+VCCA FDL VRM has high ripple voltage.	add C1867, 1uF on Vout pin of U8	A00
106	33	Sub woofer AMP Speaker AMP	2011/2/15	Compal	EOS caused Audio Amp power pin (B+) burnt [DF455411] [DF455416]	change U16/U21 pin 28, 29 from GNDA to GND	A00
107	38,39	ELC (2~3)	2011/2/15	Compal	silkscreen reversed with ME drawing because of footprint created error.	update PCB footprint of JMEDIA, JKP and rotate pin define 180°	A00
108	1~43	All	2011/2/15	Compal	short all reserved 0 Ohm resister	change footprint of all reserved 0 ohm resister to "R_short" and depop them.	A00
109	27	HDMI SW	2011/2/22	Compal	HDMI CEC capacitance EA test fail.	Add R1919, R1920, reserved for HDMI EA regression.	A00
110	27	HDMI SW	2011/2/22	Compal	HDMI EA Eye fail.	Change R1859 from 499 to 430 ohm.	A00
111	28	DP SW	2011/2/22	Compal	DP EA Eye fail.	Change R1701 from 4.99K to 3.48K ohm.	A00
112	33	Sub woofer AMP Speaker AMP	2011/2/22	Compal	Volume is lower when the first click system volume bar after SUT idle 30s [bits:DF450421]	Change R1567 from 330K to 200 ohm.	A00
113	38	ELC (2)	2011/3/1	Compal	To imrove low fail rate issue that caused of ESD which factory found during PT/ ST build.	Change Q272A/Q272B (DMN66D0LDW-7) to Q221, Q222 (SSM3K7002F)	A00
114	43	IO/B CONN / KB	2011/3/1	Compal	add new footprint of Foxconn KB connector for ME requirement.	Add JKB2, co-layout with JKB	A00
115	1~43	All	2011/3/9	Compal	Change 2N7002 due to non-ESD protection capability issue.	change SB570020110 S TR 2N7002E-T1-E3 1N SOT23 to SB000008J10 S TR 2N7002H 1N SOT23-3 PANJIT	A00

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